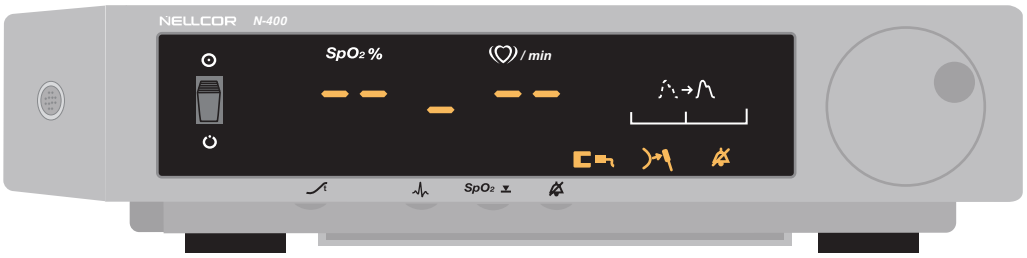
NELLCOR

N-400

Fetal Pulse Oximetry Monitor
Technical Manual



To obtain information about a warranty, if any, for this product, contact Nellcor Puritan Bennett Technical Services or your local Nellcor Puritan Bennett representative.

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Contents

INTRODUCTION

Manual Overview

This manual contains information about servicing the N-400 Fetal Oxygen Saturation Monitor. Only qualified service personnel should service this product. Before servicing the device, read the operator's manual carefully for a thorough understanding of operation.

Warnings, Cautions, And Notes

This manual uses three terms that are important for proper operation of the device: Warning, Caution, and Note.

Warning

A warning precedes an action that may result in injury or death to the patient or user. Warnings are boxed and highlighted in boldface type.

Caution

A caution precedes an action that may result in damage to, or malfunction of, the device. Cautions are highlighted in boldface type.

Note

A note gives information that requires special attention.

Device Description

The *NELLCOR PURITAN BENNETT*® Fetal Oxygen Saturation Monitor, model N-400, measures functional oxygen saturation of arterial hemoglobin ($FSpO_2$) and pulse rate in fetuses. The N-400 monitors fetal $FSpO_2$ and pulse rate noninvasively to the fetus during labor and delivery, with measurements updated at each qualified pulse.

The system consists of three components: N-400 Fetal Oxygen Saturation Monitor, N-400 Fetal Patient Module, and a *NELLCOR PURITAN BENNETT* Fetal Oxygen Sensor. The N-400 also provides analog and digital outputs for external data recording devices. The N-400 Fetal Patient Module provides initial amplification of the fetal oximetry signal. This patient module has a connector for the sensor and a cable that connects into the N-400 front panel.

The N-400 provides immediate use after power-up, without need for operator calibration. Features include:

- Automatic self-test and error messages.
- Automatic oximetry calibration
- Visible oximetry displays.

The N-400 provides the operator with the capability to tailor the operating parameters for specific clinical applications.

Capabilities include:

- Audible alarm (default state is OFF), with adjustable alarm volume.
- Operator-configured visible and audible low-saturation alarm limit (the default alarm limit is set to zero).
- An audible indicator for both $FSpO_2$ and pulse rate: a tone signals each pulse and its pitch varies with changes in $FSpO_2$. This audible indicator has an adjustable volume. (The default state of this feature is OFF.)
- Two oximetry operating modes that change measurement averaging time to suit varied clinical applications.
- Analog output of $FSpO_2$ saturation and pleth waveform data.
- Digital output of $FSpO_2$ saturation, pulse rate, pleth, and signal quality data.

Routine Maintenance

Nellcor Puritan Bennett recommends the following inspection, performance and safety checks once every two years. These checks should be performed by qualified service personnel.

Inspection Checks:

- Inspect the monitor for any mechanical and/or functional damage
- Inspect the safety relevant labels for legibility
- Inspect the fuse to verify compliance with the rated current and breaking characteristics
- Performance Checks:
- Verify that the alarms function as described in the Operator's Manual
- Using the FSpO2 Tester, Model SRC-4, verify the operation of the monitor by following the instructions in the SRC-4 Technical Manual, Guide to Operation.

Safety Checks: Using a Safety Analyzer, check the following limits:

- Ground Wire Resistance to a limit of ≤ 0.2 Ohms
- Enclosure Leakage Current in normal conditions to a limit of ≤100µAmps
- Patient Leakage Current in normal conditions to a limit of ≤20µAmps with Patient Module connected
- Patient Leakage Current in a single fault condition, Mains voltage on the applied part, to a limit of ≤100µAmps

CAUTION: Do not immerse the N-400 in liquid or use caustic or abrasive cleaners.

Cleaning

To clean the surface of an N-400, dampen a cloth with a commercial nonabrasive cleaner and wipe all monitor surfaces. Do not spray or pour liquid directly on the N-400 or its accessories. Do not allow any liquid to come in contact with the power connector, fuse holder, or switches. Do not allow any liquid to penetrate switches, connectors, or openings in the chassis.

Spare parts

Contact Nellcor Puritan Bennett Technical Services or your local Nellcor Puritan Bennett representative to obtain information about the availability of spare parts for the N-400.

Overview

This chapter discusses potential problems and suggestions for resolving them. If you experience a problem while using the N-400 and are unable to correct it, contact Nellcor's Technical Service Department or your local Nellcor representative.

Note: Several of the indicators and messages described below are specific to the N-400 monitor. Electronic fetal heart rate monitors using Nellcor FSpO2 technology may function differently from the N-400. Refer to manufacturer's documentation for details.

Potential Problems and Resolutions

1. Displayed FSpO2 does not correlate with the SaO2 value calculated from a fetal scalp blood sample measurement on a blood gas analyzer.
   - Close correlation requires simultaneous blood sampling and pulse oximeter measurements from the same arterial supply. Blood samples exposed to air during the sampling process may not accurately reflect true arterial values.
   - The SaO2 calculation may not have been correctly adjusted for the effects of pH, temperature, PaCO2, 2,3-DPG, or the presence of fetal hemoglobin. Check whether calculations have been corrected appropriately for relevant variables. (See the *Principles of Operation* chapter in the *N-400 Operator's Manual* for more information.) In general, calculated SaO2 values are not as reliable as direct CO-oximeter or pulse oximeter measurements.
   - *OxiFirst* System accuracy can be affected by incorrect sensor application or use, significant levels of dysfunctional hemoglobins, excessive patient movement, venous pulsation, or nearby electrosurgical interference. Observe all instructions, warnings, and cautions in this manual and in the *N-400 Operator's Manual*.
   - Oxygen saturation greater than 85% and/or pulse rate less than 100 bpm could indicate that the values are maternal in origin. Check sensor placement to ensure that it is properly positioned on the fetus.
2. Displayed FSpO2 does not correlate with the SaO2 value calculated from a fetal scalp blood sample measurement on a laboratory CO-oximeter.
   - Close correlation requires simultaneous blood sampling and pulse oximeter measurements from the same *arterial* supply. Blood samples exposed to air during the sampling process may not accurately reflect true arterial values.
   - Fractional measurements may not have been converted to functional measurements before the comparison was made. The N-400, as well as other two-wavelength oximeters, measures functional saturation. Multi-wavelength oximeters measure fractional saturation. Fractional measurements must be

converted to functional measurements for comparison. Refer to the equation for this conversion in the *Principles of Operation* chapter in the *N-400 Operator's Manual*.

- Oxygen saturation greater than 85% and/or pulse rate less than 100 bpm could indicate that the values are maternal in origin. Check sensor placement to ensure that it is properly positioned on the fetus.
- Check whether or not CO-oximeter values have been correctly adjusted for the presence of fetal hemoglobin.

3. N-400 does not turn on.

   - Check that the mains (AC) ON/OFF switch on the rear panel is set to ON before turning on the standby switch on the front panel. (Refer to *Turning on the N-400* on page 22.)
   - Check mains (AC) connection. Check that the N-400 is connected properly to mains (AC) supply.
   - Check that the AC voltage selector is set for the correct voltage range.
   - Check mains (AC) fuses.
   - Refer to *Turning on the N-400* section (page 22) for additional information.

4. Fetal Patient Module cannot be connected to the monitor.

   - Use only a Nellcor Fetal Patient Module.
   - Connector pins may be bent; replace with another Fetal Patient Module.

5. SENSOR UNPLUGGED indicator is on or the red sensor emitter is not lit.

   - Check connection between the sensor and the patient module.
   - Check connection between patient module cable and front panel of monitor.
   - If all connections are okay, try a new sensor.
   - If problem persists, try a new Fetal Patient Module.
   - If problem persists, contact Nellcor's Technical Service Department or your local Nellcor representative.

6. Fetal heart rate slows during, or immediately following, sensor placement.

   - A fetal response to stimulation could cause a reflex bradycardia.

Caution: If the fetal heart rate slows during vaginal exam or sensor insertion, stop the procedure. Do not proceed with sensor placement as this can cause a reflex bradycardia stimulus. Wait for the fetal heart rate to return to the previous range before proceeding.

7. SENSOR LIFTED indicator remains ON or FLASHING, even though appropriate adjustments have been made.

   - Sensor is not making adequate contact at the sensor site on the fetus.
   - If the indicator is ON and AdJ SEn is being displayed, the sensor may be floating in amniotic fluid.
   - If the indicator is FLASHING and AdJ SEn is being displayed, the sensor may be covered with vernix. If condition persists, remove the sensor and check for vernix in the fluid channel.

- If the indicator is ON and AdJ SEn is **not** being displayed, the sensor may be in the vagina.
- Assess sensor depth relative to the station of the fetal head. Advance or withdraw the sensor as indicated in the *Preparation for Sensor Placement* and *Sensor Placement and Adjustment* chapters in this manual.
- As the head descends, the sensor should also descend. If the sensor has not descended, as indicated by the centimeter mark at the introitus, withdraw the sensor in 1-cm increments until contact is again achieved, noting the cm mark on the stylet chamber relative to introitus.
- Refer to the *Appendices* in this manual for additional information.
- If the indicator does not respond to advancing, withdrawing, or reorienting the position of the sensor, the sensor may be damaged. Remove it and place a new sensor.

8. SEARCHING indicator is on; PULSE AMPLITUDE appears to indicate pulses, but there is no FSpO2 or pulse rate displayed. Additionally, the AdJ SEn message may be displayed.

   - Assess fetal status.
   - The signal quality is below the acceptable threshold requirement necessary to post data on the display. Utilize the audible PULSE TONE feature to help assess the signal quality.
   - Excessive maternal or fetal patient motion may be interfering with signal quality. If possible, keep the mother still.
   - A uterine contraction may be interfering with signal quality. Wait for the contraction to subside to see if previously displayed values return.
   - The fetal perfusion may be too low for the N-400 to consistently detect an acceptable pulse.
   - Assess sensor depth relative to the fetal presenting part; advance or withdraw the sensor as indicated in the *Preparation for Sensor Placement* and *Sensor Placement and Adjustment* chapters in this manual.
   - Refer to the *Appendices* in this manual for additional information.
   - If SEARCHING indicator continues to display after evaluations and adjustments have been made:
     - The sensor may be damaged; replace it.
     - The patient module may be damaged; try another Fetal Patient Module.

9. AdJ SEn message remains displayed and SEARCHING and SENSOR LIFTED indicators are OFF.

   - The sensor may be over hair or other light-absorbing surface.
   - Assess sensor depth relative to the station of the fetal head. Advance or withdraw the sensor as indicated in the *Preparation for Sensor Placement* and *Sensor Placement and Adjustment* chapters in this manual.
   - Assess sensor position relative to orientation of fetal head. If necessary, reorient the sensor position as indicated in the *Preparation for Sensor Placement* and *Sensor Placement and Adjustment* chapters in this manual.
   - Refer to the *Appendices* in this manual for additional information.

- If the indicator does not respond to advancing, withdrawing, or reorienting the position of the sensor, the sensor may be damaged. Remove it and place a new sensor.

10. $FSpO_2$ or pulse rate change rapidly; PULSE AMPLITUDE indicator is erratic.

- Assess fetal status.
- Excessive maternal or fetal patient motion may be making it impossible for the N-400 to find a pulse pattern. If possible, keep the mother still.
- Check whether the sensor is positioned properly on the fetus, and reposition it if necessary.
- Set the N-400 response time for Mode 1.
- A nearby electrosurgical unit (ESU) may be interfering with performance.

WARNING: The *OxiFirst* System should not be used while using an Electrosurgical Unit (ESU). Remove the fetal oximetry sensor from the mother and fetus before using an ESU. An improperly grounded ESU can cause surface skin burns on the fetus if both the *OxiFirst* System and an ESU are used together.

11. Displayed pulse rate does not agree with that of an electronic fetal heart rate monitor.

- Excessive maternal or fetal patient motion may be making it impossible for the N-400 to find a pulse pattern. If possible, keep the mother still.
- Check fetal heart rate by auscultation.
- Ensure that the sensor is properly positioned on the fetus.
- Oxygen saturation greater than 85% and/or pulse rate less than 100 bpm could indicate that the values are maternal in origin. Check sensor placement to ensure that it is properly positioned on the fetus.

12. $FSpO_2$ saturation > 85%.

- The sensor may be facing the uterine wall and may be reading maternal saturation. Confirm that the sensor is positioned correctly against the fetus.
- The sensor has white markings on both sides. The side with numbers at 1-cm intervals (30, 29, 28, 27…) should be facing toward the fetus. The side with numbers only at 17, 20, 25, 30 is the maternal side and should be facing away from the fetus.
- Palpate the maternal pulse and compare it to the heart rate displayed on the fetal heart rate monitor and to the pulse rate displayed on the N-400 monitor. If the maternal pulse matches the N-400 displayed pulse rate, sensor is most likely monitoring maternal oxygen saturation. Reposition or adjust the sensor.
- Normal sensor operation may be affected by maternal pulsations or vernix in the fluid channel. Withdraw the sensor in 1-cm increments to better position the sensor; hold in place for 15 seconds.

- If still unsuccessful in correcting this condition, completely withdraw sensor and inspect for vernix in the fluid channel.

Error Codes

Table 1 lists error codes, their probable cause, and recommended action.

Table 1: Error Codes

Error Code	Probable Cause	Recommended Action
ERR 1	Line Voltage selection incorrect; or RAM chip failure.	If changing the Line Voltage selection does not correct the error, contact NPB Technical Services.
ERR 2	ROM Failure; Defective Memory	Contact NPB Technical Services
ERR 3	Defective display segment or indicator	The error can be cleared by pressing any front panel button. Contact NPB Technical Services.
ERR 4	Clock battery failure. Will occur during the installation of new PROMs.	While installing new PROMs, the error can be cleared by pressing any front panel button. If the error occurs in the field, contact NPB Technical Services.
ERR 5	Communications failure. UART failure during Power On Self Test (POST).	The error can be cleared by pressing any front panel button. In the field, contact NPB Technical Services.
ERR 6	Clock battery failure. May occur during the installation new PROMs.	While installing new PROMs, the error can be cleared by pressing any front panel button. If the error occurs in the field, contact NPB Technical Services.
ERR 7	A front panel button is stuck or held in position during the monitor POST.	Check all front panel buttons for proper operation. If the error does not clear, contact NPB Technical Services.
ERR 8	Line Voltage selection is not the same as the AC supply voltage.	Change line voltage selection.
ERR 9	Memory Failure or a Processor 80C186 problem.	Contact NPB Technical Services
ERR 10	Memory Failure or a Processor 80C186 problem.	Contact NPB Technical Services
ERR 119	ROM run-time failure (Memory Failure)	Turn the ON/Standby Switch to *Standby* and the mains ON/OFF switch to OFF. Turn back to ON after 5 seconds. If error is not cleared, contact NPB Technical Services.

Table 1: Error Codes

ERR 120	RAM run-time failure (Memory Failure)	Turn the ON/Standby Switch to *Standby* and the mains ON/OFF switch to OFF. Turn back to ON after 5 seconds. If error is not cleared, contact NPB Technical Services.
ERR 121	Clock Failure.	The error can be cleared by pressing any front panel button. In the field, contact NPB Technical Services.
ERR PB	Internal communications problem.	Turn the ON/Standby Switch to Standby and the mains ON/OFF switch to OFF. Turn back to ON after 5 seconds. If error is not cleared, contact NPB Technical Services.
ERR SEN	The sensor is not compatible with the system configuration.	Replace with the correct sensor.

The error codes in Tables 2 and 3 are for information use only by NPB Technical Services personnel and are divided into two categories.

INFORMATIONAL—The instrument continues to operate, but does not post numbers. The ERR code may be cleared with the push of any front panel button and it would be desirable for the clinician to record the ERR number for our information.

OPERATIONAL—The instrument stops posting numbers, shuts down the LEDs and must be reset by turning the Mains AC Switch OFF and then ON again after approximately 5 seconds. It is also desirable to record the ERR number for information purposes

Table 2: Informational—Service Only

Error Code	Probable Cause	Instructions
ERR 122	Software ring buffer supporting external communications is filled. Data may be discarded.	Slow running Processor clock, or a memory problem, or an internal software error. See above for clearing of error.

Table 3: Operational—Service Only

Error Code	Probable Cause	Instructions
ERR 101, 201, 301, 401, 501, 802	IPC Get Long Message Buffer, Internal Error, Buffer Starvation	Slow running Processor clock, or a memory problem, or an internal software error. See above for clearing of error.

Table 3: Operational—Service Only (Continued)

ERR 102, 203, 302, 402, 503	IPC Invalid Message	See ERR 101
ERR 103, 104, 105, 205, 305, 404, 505, 601, 801	IPC Send	See ERR 101
ERR 106, 206, 306, 406, 506	IPC Reply	See ERR 101
ERR 107, 207, 307, 407, 507	IPC Queue Create	See ERR 101
ERR 108, 208, 308, 408, 508	IPC Receive	See ERR 101
ERR 109	RTDIAG: Ping Failure	S/W Failure
ERR 110	RTDIAG: Told to halt via IPC message (test hook)	S/W Failure
ERR 112	RTDIAG: Interrupt vector error	See ERR 101
ERR 113	POST: Bad A/D start	A/D converter problem
ERR 114	RTDIAG: Stack check	S/W Failure or may be a bad memory chip
ERR 115	Non-volatile log error in the Header format	S/W Failure or Smartwatch
ERR 116	Non-volatile log error in the Data	S/W Failure or Smartwatch
ERR 117	Release of a long message buffer	S/W Failure
ERR 202	IPC Release Long Message Buffer	See ERR 101
ERR 209, 511	Invalid Parameter	See ERR 101
ERR 210	Invalid Offset	See ERR 101
ERR 211	No Ping Message	See ERR 101
ERR 409, 502	Release Long Message Buffer	See ERR 101
ERR 512	Invalid SpO2 Mode	See ERR 101
ERR 602	TIMER_INV_MSGINIT	S/W Error
ERR 603	TIMER_INV_RESTART	S/W Error
ERR 604	TIMER_INV_CANCEL	S/W Error
ERR 701	IPC Send Error	See ERR 101
ERR 702	IPC Get Long Message Buffer	See ERR 101
ERR 703	Internal programming error in devices programming	S/W Error

Table 3: Operational—Service Only (Continued)

ERR 704	Invalid data to a case statement. Default executed.	S/W Error
ERR 705	A/D Overrun	A/D chip failure
ERR 803	IPC Release Long Message Buffer, Internal Error, corrupt pointer	S/W Error
ERR 804	IPC Routing Problem - Destination CPU incorrect	S/W Error
ERR 901	Interrupt occurred SYS_DIVIDE_0	S/W Error
ERR 903	Interrupt occurred SYS_INVALID_OPCODE	H/W Error; Bad memory or memory controller
ERR 904	Interrupt occurred SYS_INVALID_INT	H/W Error; Bad memory or memory controller
ERR 905	Assert macro SYS_ASSERT	S/W Error
ERR 906	Internal coding error in IPC SYS_XRECV_TIMEOUT	S/W Error
ERR 907	RTXC returned an error SYS_RTXC	S/W Error
ERR 908	Non-volatile log memory integrity failure	H/W Error; Smartwatch failure.
ERR 999	Could not convert the major and minor error codes to a number between 0 and 998	S/W Error

PACKING FOR SHIPMENT

General Instructions

Should you need to ship the N-400 monitor for any reason, first contact Nellcor Puritan Bennett Technical Services for a returned goods authorization (RGA) number. Mark the shipping carton and any shipping forms with the RGA number.

Pack the monitor carefully. Failure to follow the instructions in this section may result in loss or damage not covered by the Nellcor Puritan Bennett warranty. If the original shipping carton is not available, use another suitable carton or call Nellcor Puritan Bennett Technical Services to obtain a shipping carton.

Repacking In Original Carton

If available, use the original carton and packing materials. Pack the monitor as follows:

1. Place the monitor and, if necessary, accessory items in original packaging.
2. Place in shipping carton and seal carton with packaging tape.
3. Label carton with shipping address, return address, and RGA number.

Repacking In A Different Carton

If the original carton is not available:

1. Place the monitor in plastic bag.
2. Locate a corrugated cardboard shipping carton with at least 200 pounds per square inch (psi) bursting strength.
3. Fill the bottom of the carton with at least two inches of packing material.
4. Place the bagged unit on the layer of packing material and fill the box completely with packing material.
5. Seal the carton with packing tape.
6. Label carton with shipping address, return address, and RGA number.

Performance

Display Ranges:

Pulse Rate: 0 to 250 beats/minute

FSpO2: 0% to 100%

Accuracy:

Pulse Rate: 30 to 240 beats/minute, ±3 bpm

FSpO2 Calibration and Reproducibility:

Calibration of the *NELLCOR PURITAN BENNETT* N-400 Fetal Oxygen Saturation Monitor was accomplished through controlled hypoxia studies in a piglet model. The calibration was validated in an independent animal study of a different group of piglets and in a multi-center human study comparing N-400 readings to simultaneous laboratory arterial blood saturation values obtained on severely cyanotic human infants and children.

Reproducibility of system was evaluated under conditions of actual use in a series of dual sensor studies, in which two sensors were placed simultaneously on a human fetus during active labor.

The resulting reproducibility was 1 SD = 6.0%. Nominally, 68% of the measurements across the population will be within ±1 SD (standard deviation).

Sensor:

Type:*NELLCOR PURITAN BENNETT* Fetal Oxygen Sensor (reflectance sensor)

Heating: Sensor power dissipation is less than 80 mW total heat dissipation by LEDs (less than 3.0°C temperature rise).

Controls

Front Panel: ON/STANDBY switch, control knob, Audio Alarm Off button, Low Saturation Limit button, ECG Display button, Response Time button

Rear Panel: Mains (AC) ON/OFF switch, Decrease (zero) button, Increase (full-scale) button, DIP switches (used to set analog output scale, RS-232 format, and baud rate)

Alarms

The audible alarm default state is OFF. Audible and visible alarms for low oxygen saturation; audible alarm and visual indicators for loss of pulse. Audible alarms are interrupted briefly for detected pulses; the volume is adjustable. See *Alarms* in the N-400 operator's manual.

AUDIO PULSE

Default volume is OFF. If enabled, and a signal from the sensor is present, an audible beep sounds with each detected pulse; volume is adjustable with control knob; pitch varies to reflect changes in oxygen saturation.

RESPONSE MODES

Two response modes, selected by the Response Time button: Mode 1 (default), slow, 50 seconds (at 150 bpm); Mode 2, fast, 11 seconds (at 150 bpm). See Response Time in the *Guide to Operation* section of the N-400 operator's manual.

ECG

Via rear-panel ECG input jack

- Input: High-level ECG output signal from EFM through an ECG interface cable. For optimum performance, a signal with positive deflection is recommended.
- Input Range: 0.05 V minimum input signal; should not exceed ±15 V. Minimum of 10 ms wide at 50% of peak amplitude.

SWITCHES

Ten for digital output format and analog output voltage range.

Switch Section	Function
1	analog output voltage range
2,5,9,10	not used
3,4	baud rate select
6,7,8	RS-232 format

DATA I/O

Digital

Type:	RS-232 format
Connector:	9-pin D-type, female
Baud Rate:	Switch-selectable, 1200, 2400, 9600, and 19,200
Formats:	Conversation, beat-to-beat

Analog

3 each; 3/32-inch subminiature phone jacks

Outputs:	$FSpO_2$ and Plethysmographic Waveform
Voltage:	0-1 or 0-10 V (switch-selectable, DIP switch 1) Maximum voltage output: 10 V
$FSpO_2$ Accuracy:	±20 mV at zero (0), ±0.5% of full scale, referred to front panel display
Input:	High-level ECG output signal from an EFM

Connectors

Front Panel:	N-400 Fetal Patient Module Connector
Rear Panel:	$FSpO_2$ analog output jack (3/32”) Plethysmographic Waveform analog output jack (3/32”) Fetal High-level ECG input jack (3/32”) Serial Communications connector (9-pin, D-type connector) Mains (AC) power input

Electrical

Voltage Requirement:	100 – 120 V~ ±10% at 50/60 Hz 200 – 240 V~ ±10% at 50 Hz
Current Requirement:	300 mA, maximum
Power Consumption:	Maximum rating: 30 VA
Fuses:	115 V~: 2 x T 500 mA, 250 V 230 V~: 2 x T 250 mA, 250 V
Classification:	Protective Class: IEC Class I Degree of Protection: Type BF Enclosure Degree of Protection: Ordinary (IPXO) Mode of Operation: Continuous

PHYSICAL

Monitor

Dimensions: 12.6” wide x 12” deep x 3” high
(32 cm x 30 cm x 8 cm)

Weight: 9 lb
(4.1 kg)

Patient Module

Cable length: 13 ft (4 m) cable

Connectors: Lemo B-series, mates with 12-pin connector on N-400 front panel; Fetal Sensor connector, mates with 9-pin connector on Fetal Oxygen Sensor

Environmental

Transport (in shipping container)

Temperature: –40°C to +70°C (–40°F to +158°F)

Altitude/
Barometric Pressure: –390 m to +6,096 m (–1280 ft to +20,000 ft)

+1060 hPa to +500 hPa (+31.1 in. Hg to +14 in. Hg)

Relative Humidity: 15% to 95% (noncondensing)

Storage (not in shipping container)

Temperature: –40°C to +60°C (–40°F to +140°F)

Altitude/
Barometric Pressure: –390 m to +6,096 m (–1280 ft to +20,000 ft)

+1060 hPa to +500 hPa (+31.1 in. Hg to +14 in. Hg)

Relative Humidity: 15% to 95% (noncondensing)

Operating

Temperature: +5°C to +40°C (+41°F to +104°F)

Altitude/
Barometric Pressure: –390 m to +6,096 m (–1280 ft to +20,000 ft)

	+1060 hPa to +500 hPa (+31.1 in. Hg to +14 in. Hg)
Relative Humidity:	15% to 95% (noncondensing)

Emissions Compliance

EN55011 Emissions Classification

CISPR II, Group I, Class B

This section contains the following technical information:

- Theory of Operation
- Block Diagram Analysis
- Circuit Descriptions
- Schematic, Part Locator, and Block Diagrams

THEORY OF OPERATION

Operation of the N-400 Fetal Oxygen Saturation system is based on the principles of pulse oximetry, which in turn is based on spectrophotometry and plethysmography. The system includes an electro-optical sensor and a microprocessor-based monitor.

Oxyhemoglobin and deoxyhemoglobin have different light absorption characteristics in the far red and infrared wavelength spectrums. Less red light is absorbed by oxyhemoglobin than by deoxyhemoglobin. Relatively more infrared light is absorbed by oxyhemoglobin than by deoxyhemoglobin. Arterial blood in a well-oxygenated fetus will typically contain a higher concentration of oxyhemoglobin than deoxyhemoglobin.

The N-400 uses these differences in the absorption of far red and infrared light by oxy- and deoxyhemoglobin to determine fetal oxygen saturation by measuring the change in light levels caused by pulsating arterial blood in the tissue.

The fetal oxygen sensor has two low-voltage light-emitting diodes (LEDs). One of these LEDs emits red light (nominal 735 nm wavelength) and the other emits infrared light (nominal 890 nm wavelength). When the sensor has been properly positioned on the fetal temple or cheek, light from each of these LEDs is alternately sent through the fetal skin into the underlying tissues at the sensor site. The amount of light absorbed by the tissue or blood underlying the fetal sensor is determined from the amount of light that scatters back to the tissue surface and is picked up by the photo detector (photo diode) on the sensor.

Light absorption is first measured by the N-400 at each wavelength when no pulsatile blood is present. This reflects the background light absorption of bone, tissue, and venous blood, which are generally considered non-pulsating. This measurement is analogous to the reference measurement of a spectrophotometer.

With each fetal heart beat, a pulse of arterial blood flows to the oxygen sensor site. Red and infrared light absorption are then measured by the N-400 at each wavelength when this pulsatile, arterial blood is in the tissue. The N-400 microprocessor compares the background light absorption measurements to the absorption measured at both

light wavelengths during each arterial pulse. The ratio of the corrected absorption at each wavelength is used to determine fetal oxygen saturation ($FSpO_2$).

Auto Calibration

The N-400 oximetry subsystem is automatically calibrated each time the monitor is turned on, at periodic intervals thereafter, and whenever a new sensor is connected. The intensities of the sensor LEDs are adjusted automatically to compensate for differences in tissue light absorption characteristics, or other sources of light attenuation.

Each fetal oxygen sensor is calibrated when manufactured: the effective mean wavelength of the LEDs is determined and encoded into a calibration resistor in the sensor. The N-400 software reads this calibration resistor when the sensor is connected to determine the appropriate calibration coefficients for the measurements obtained by that specific sensor.

Functional vs Fractional Saturation

Because the N-400 measures functional SaO_2, it may produce measurements that differ from those of instruments that measure fractional SaO_2. Functional SaO_2 is oxygenated hemoglobin expressed as a percentage of the hemoglobin that is capable of transporting oxygen. Because the N-400 uses two wavelengths, it measures oxygenated and deoxygenated hemoglobin, yielding functional SaO_2. It does not detect dysfunctional hemoglobins, such as carboxyhemoglobin or methemoglobin.

In contrast, some laboratory instruments such as the Instrumentation Laboratory 282 or 482 CO-Oximeter report fractional SaO_2 - oxygenated hemoglobin expressed as a percentage of all measured hemoglobin, whether or not that hemoglobin is available for oxygen transport. Measured dysfunctional hemoglobins are included.

Consequently, to compare N-400 measurements directly with those of another instrument, that other instrument must measure functional SaO_2. If the other instrument measures fractional SaO_2, those measurements can be converted to functional SaO_2 using the following equation.

$$\text{functional saturation} = \frac{\text{fractional saturation}}{100 - (\%\ \text{carboxyhemoglobin} + \%\ \text{methemoglobin})} \times 100$$

Measured vs Calculated Saturation

When SaO_2 is calculated from a blood gas measurement of the partial pressure of arterial oxygen (PaO_2), the calculated value may differ from the N-400 $FSpO_2$ measurement. This is because the calculated SaO_2 may not have been corrected for the effects of variables that shift the relationship between PO_2 and SO_2 (see Figure 1): temperature, pH, the partial pressure of carbon dioxide (PCO_2), and the concentrations of 2,3-DPG and fetal hemoglobin.

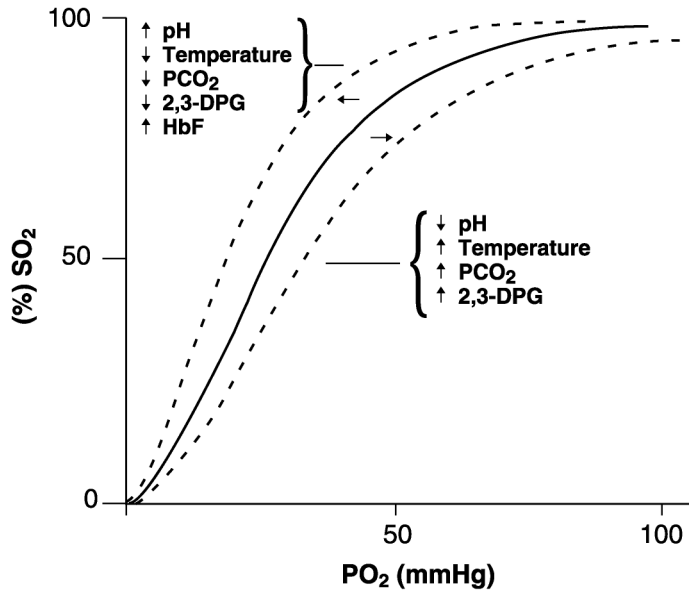


Figure 1: Oxyhemoglobin Dissociation Curve

Block Diagram Analysis

The following discussion analyzes the N-400 major circuit levels using block diagrams. Refer to the overall block diagram on the foldout pages at the end of this section.The circuits and components of the N-400 system are divided into two major functional blocks: patient circuits and communication circuits.

The terms “patient circuits” and “communications circuits” refer to the physical parts of an N-400 system and define the electrical safety characteristics of the monitor. Circuits in the patient block are electrically isolated from those in the communications block to provide maximum protection for both patient and user. The block diagram illustrates the relationship of these divisions.

Patient Circuits

Block diagram analysis of the circuits in the patient block focuses on the pulse oximetry or oxygen saturation channel signal path from the patient sensor site to the front-panel display. The discussion presents digital circuits as processing support circuits for oxygen saturation channel and the bi-directional optical communication channels to the Communications Circuits Section.

AC Power Input

Operating power for both patient and communications sections comes from the AC mains through a connector and line filter assembly, two line fuses, a line voltage selector switch and into the primary coil of the power transformer, T1. This transformer has three isolated secondary circuits: one for the communications section operating power and two that provide isolated 9.2 and 12.5 VAC for the patient circuits.

Power Control

The power control circuits are located in the patient section on the Power PCB. This circuit uses a FET to separate system and power grounds, providing software control of the system power configuration. The circuit also includes watchdog capability for unacceptable system operation parameters.

Power Supplies

The module has two separate power supplies on the Power PCB. Both supplies are pulse-width-modulated. There is a +5V supply and a ±18V supply.

Pulse Oximetry FSpO$_2$ Channel

The oxygen saturation signal is developed by a Nellcor Puritan Bennett (NPB) Fetal Oxygen Sensor applied to the fetus. Using LEDs, the sensor generates alternate IR and Red energy pulses at the measurement site. A photodiode responds to the pulse-modulated energy. The photodiode output, called the oxygen saturation signal, is electrically coupled into the patient module. The signal is then converted from a current to a voltage, conditioned, and coupled through the patient module cable to a connector on the monitor front panel.

The oxygen saturation signal is then coupled from the front panel connector through a cable assembly to an input amplifier (INAMP) on the Processor PCB. Circuits in the INAMP facilitate the microprocessor-controlled gain adjustment and present the gain-conditioned signal to a synchronous detector.

Synchronous detection further conditions the signal in a manner that allows pulse waveform recovery with minimal artifacts. The detected signal is then passed through microprocessor-controlled gating circuits that demultiplex or separate the Far Red and IR components and direct them to appropriate filter/amplifiers, one for Far Red and one for IR. The Far Red and IR filter/amplifier channels consist of active low-pass filters (DC to 8Hz) that recover and amplify the low frequency, or the pulse waveform component of the oxygen saturation signal.

The outputs of the filter/amplifier circuits are signals containing pulse waveforms, one from the Far Red and one from the IR channel. The relative amplitude of these waveforms provides the information necessary to calculate oxygen saturation and pulse rate. The pulse waveforms are then sequenced through a multiplexer, conditioned, measured, and digitized.

Measurement Circuits

The oxygen saturation signals, sensor contact signal, and housekeeping data are multiplexed, and measured by a 16-bit analog-to-digital converter. Calculations are made by the microprocessor, and the monitor displays the results—oxygen saturation and pulse rate.

Display Circuits

The N-400 display circuits are located on the Display PCB attached to the front panel. The circuits include display drivers and LED display devices for oxygen saturation, pulse rate, signal quality, pulse amplitude, and status indicators. Interface circuits on the front panel allow operator control through push buttons and the control knob.

Digital Support Circuits

All digital support circuits reside on the Processor PCB and include the microprocessor, ROM, RAM, and associated control and timing components, and communication components. These circuits control the bi-directional optical communication link to the communications section.

User Interface Circuits

The front panel push buttons and control knob signals originate on the Display PCB. These circuits communicate directly with the microprocessor through the data bus.

Communications Circuits

The block diagram analysis of circuits in the communications section focus on the analog and digital I/O communication channels and user interface capability. Digital circuits are discussed as processing support circuits for the communication channels and user interface.

AC Power Input

The operating power for the communications section comes from an isolated transformer secondary that provides isolated 7.5 VAC.

Power Supply

Three power supplies located in the communications section provide power for the communications circuits. An AC input of approximately 7.5V rms is rectified and filtered and applied to regulator and DC-to-DC converter circuits that provide +5V, , +12V, –12V, +15V and –15V.

Analog Channels

Analog circuits process ECG, SATURATION, and PLETHYSMOGRAPH. The circuits consist of a sample-and-hold circuit for SAT and PLETH analog output signals and an ECG input circuit for external ECG monitor high-level input.

Note: The PLETH waveform (low resolution, autoscaled) is not intended for any diagnostic purpose.

Digital Channels

The digital circuits include communications circuits for internal N-400 communications between the patient and communications circuit blocks, and for RS-232 data output to external printers or digital devices.

User Interface

The user interface consists of ZERO and FULL push button switches for calibrating external strip-chart recorders. These rear-panel switches generate zero- and full-scale (user-selectable between 1V or 10V) voltage on the $FSpO_2$ and Pleth analog outputs. Also, there is a multi-section slide switch that controls serial data baud rate and format, and analog output voltage range.

Circuit Descriptions

Refer to the fold-out pages at the end of this manual for the instrument schematic diagrams. The major circuit sections consist of:

- The Fetal Patient Module
- The Processor PCB—Patient Isolated circuitry
- The Processor PCB—Data Communications circuitry
- The Front Panel Display circuitry (Display PCB)
- The Power Supply

Throughout this section and on the schematic diagrams, active low logic signals are designated by an asterisk after the signal name (for example, SIGNAL*).

Fetal Patient Module Description

The High Gain Patient Module contains a current to voltage (I:V) converting amplifier for the detector signal from the sensor. It also provides throughput for emitter, Rcal, and contact signals.

Connections

Detector (**DETECTOR CATHODE**, **DETECTOR ANODE**), Rcal (**RCAL**, **RCAL RET**), LED (**LED+**, **LED–**) and Contact (**SENSORUP+**, **SENSORUP–**) signals are fed through a modified 9-pin sub-miniature “D” sensor input connector to a flex circuit which is soldered to the PCB. The PCB is soldered to the Patient Module Cable which plugs into the N-400 through a 12-pin connector.

Power Conditioning

Power and ground (±15V, AGND) are provided by the N-400. Capacitor values of 1.5µf (C1, C5) and 0.1 µf (C3, C4), provide for local bypass filtering. The ground to the sensor shield is provided by a 33µf Capacitor (C6). This capacitor AC couples the shield to patient ground to prevent any DC currents from flowing through the shield to ground. The voltage created across the Rcal resistor in the sensor is locally filtered with a 0.1µf Capacitor (C8).

Detector Amplification

The sensor detector photodiode current is differentially amplified to maintain common mode rejection of interfering frequencies that may couple into the detector signal. Two low offset operational amplifiers (U1) convert the detector current signal to a voltage with a combined differential gain of 998k (two times 499k). The two 499k resistors (R1, R2) are selected as pairs matched to within 0.02% of each other in order to maintain common mode rejection. Feedback capacitors (C2, C7) provide low-pass filtering with a corner frequency of 14.5kHz. The capacitor tolerance of 1.0% was chosen for good high-frequency common-mode rejection.

The output of the two op amps are fed into a programmable instrumentation amplifier (U2) to change the differential voltage signal into a negative single-ended voltage output. A 12.7k resistor (R3) sets the programmable gain of this stage to 4.89X.

The combined I:V gain of the Patient Module is 4.88V/µA (998k X 4.89).

Processor PCB - Patient Isolated Circuitry

The Patient Isolated section of the Processor PCB contains the main oximetry electronics. This section communicates with the Display PCB, sends and receives Sensor signals, provides Power Supply PCB control, and communicates with the Communication section.

Power for this section is provided by the Power Supply PCB through a 5-pin connector (P3). Power supply control signals are provided through a 10-pin dual inline flat cable connector (P1). Sensor signals to and from the Patient Module, as well as power to the Module (through the Internal Patient Cable), are provided through a 14-pin dual inline flat cable connector (J7).

Input/Output signals for the Display PCB are provided through a 14-pin dual inline flat cable connector (J8). Speaker signals are provided through a 2-pin connector (J16). Serial communications to the Communications section are through two opto-isolators (U21, U23).

The +5 Volt power for the digital circuitry comes directly off the Power Supply PCB. A 22µf capacitor (C134) provides filtering at the power input connector (P3). Local filtering is performed by 0.047µf capacitors distributed across the board. The digital power and ground are supplied via internal PCB planes.

The Processor PCB receives ±18 Volt supplies from the Power Supply. Local filtering is provided by 10µf (C132, C131) and 0.047µf (C321, C322) capacitors. The ±18 volt supplies are down-regulated to ±15 Volts with linear regulators (VR8, VR7). This post-regulation helps remove voltage spikes on the analog supplies occurring at the switching frequency of the power supply. Local filtering is performed by .01µf (C301, C304) and 0.047µf capacitors distributed across the board. The ±15 Volts analog power is supplied via internal power and ground planes.

Certain components in the analog circuitry require ±5 Volt supplies. These are provided via additional linear regulators (VR6, VR5), which down-regulate the ±15 volt supplies.

The power input connector (P3) provides separate inputs for Digital and Analog grounds. Each ground is supplied to the circuitry via separate ground planes. The ground planes are connected at the Four Channel Digital-to-Analog Converter, or DAC, (U66) by jumper W10. This jumper is strapped on the PCB. Another jumper (W7) provides an alternative connection for the two ground planes at the Analog-to-Digital Converter (U46), but is not strapped on the PCB, nor is it to be installed in normal operation.

Digital Subsystem

MICROPROCESSOR

The Patient Isolated section of the Processor PCB uses microprocessor, U83. This microprocessor currently uses a 20 MHz crystal (Y2), yielding a bus rate of 10 MHz. The system is designed to accommodate crystal frequencies up to 30 MHz without requiring an external wait-state generator.

The RESET* signal to the microprocessor is generated by an R-C network (R115, C212) connected to the preset input of a flip-flop (U79). The time constant of the R-C network is approximately 100mS. The clock signal to the flip-flop is provided by **AC_INT**, which is derived from the 50/60 Hz AC Mains line frequency. The output of the flip-flop is held low until C212 charges enough to release the preset condition, then the output goes high on the next clock pulse. The flip-flop helps buffer the more slowly changing charge characteristics of the passive R-C network, insuring that the reset to the microprocessor is snapped quickly and cleanly. A diode (CR28) connected in parallel with the resistor provides a rapid discharge pathway for the capacitor during power-down.

The microprocessor RESET output signal is used to reset the UART (U84). The signal is inverted (U71) to provide a low true reset signal to the Analog MUX (U28), and the Analog-to-Digital Converter (U46).

ADDRESS LATCHES

Two 10-bit buss drivers (U73, U77) latch the current address onto the address buss A<16..0> when ALE is asserted from the microprocessor.

MEMORY

The Patient Isolated section uses two PROMs (U74, U82) for a total code space of 128k-bytes. The system also uses two Static RAMs (U69, U72), one of which (U69) is mated to a Smartwatch socket that provides clock/calendar functions. The Smartwatch socket has a 3-Volt Lithium battery that provides non-volatile operation for the clock/calendar as well as the RAM mated to it; thus, half, but only half, of the memory (the even RAM addresses) is saved upon power-down.

CHIP SELECTS

The chip select lines of the microprocessor act only as address decoders. Several of the ICs used in the microprocessor design require a chip enable signal that is a combination of a decoded address and a read or write strobe (or both) to ensure proper setup and hold times for data being read from or written to these devices. The chip selects will be discussed as PROCESSOR CHIP SELECTS and EXTERNAL CHIP SELECTS separately.

PROCESSOR CHIP SELECTS

The microprocessor has 13 built-in chip select lines: LCS*, UCS*, MCS0-3*, and PCS0-6*; all are active low.

LCS* (Lower Chip Select) is used to select the RAM memory. Since RAM accesses may be in either bytes or words, separate RAM IC decoding must be employed to avoid corrupting data during byte-wide write cycles. The LCS* signal is logically OR'd (U68) with address line A0 to generate the chip select signal LOW BYTE SELECT* for the "even address" RAM. The LCS* signal is OR'd (U68) with the BHE* (Bus High Enable) line to generate the chip select signal HIGH BYTE SELECT* for the "odd address" RAM.

UCS* (Upper Chip Select) is used to select the ROM memory. Since read-only memory data is only read as a word, no unique decoding is required for the two ROM ICs.

MCS2* (Midrange Chip Select 2) is used to interface with the UART (U84). The signal is referred to as UART_CS*.

The rest of the system chip selects are generated with the PCS lines (Peripheral Chip Select) of the microprocessor (PCS0-6*). PCS1* (AD_START*) initiates an Analog-to-Digital (A/D) conversion by the A/D Converter (U46), while clearing the two shift registers (U57, U59) of their previous contents. PCS4* (TIMER_CS*) selects the Timer/Counter (U80). TIMER_CS* is also used in the Pattern Generator circuitry.

EXTERNAL CHIP SELECTS

PCS5* (DECODER_CS*) enables an external address decoder to be used to generate External Chip Selects as described below.

These chip selects are generated by an external address decoder (U62) whose outputs are enabled only when PCS5* is asserted and either the RD* or WR* signal from the microprocessor are active. The RD* and WR* are logically NANDed (U61) to produce a high true enable to the decoder if either signal is active. The decoded outputs are, in order from lower to higher addresses:

INAMP_CS*: Selects the FSpO2 programmable input attenuator (U43).

ADC_READ*: Puts the value of the last 16 bit A/D conversion on the microprocessor bus through two shift registers (U57, U59).

ANALOG_MUX_CS*: Selects the Analog Multiplexer (MUX) chip (U28) in the A/D subsystem.

DAC_WR*: Selects the Digital to Analog Converter (DAC) (U66) used to set LED intensities and speaker volume.

STATUS_RD*: Puts the status flags and jumper information on the microprocessor bus through buffer (U85) and latch (U58).

DISPLAY*: Enables the selection of the display drivers on the Display PCB.

OUTPUT_CS*: Selects the output latch (U81) used to set the Pattern Generator pattern, enable the speaker, reset the watchdog timer, select the ADC channel, and select the INAMP post-DAC amplifier gain.

RESET*: Normally unused. Refer to the RESET* description above.

TIMERS/COUNTERS

The microprocessor has three built-in timers. Timer 0 generates a 50 kHz square wave signal, SENSOR_UP_CLK, which is used to determine sensor contact with the fetus. Timer 2 is an internal timer used to generate a 400Hz (2.5ms) real-time interrupt. Timer 1 is not used.

EXTERNAL TIMERS

Additional timer outputs are provided by the Timer/Counter IC (U80). Timer outputs 0 and 1 are used together to generate the clock signal, PG_CLK, that is used by the Pattern Generator circuitry.

Timer output 2 is used to generate the TONE signal used by the speaker. This output is enabled by the TONE_GATE signal from the output latch (U81). When

a timer output is disabled, the output goes high. Because of this, the TONE output signal is inverted (U71), which ensures that the speaker drive circuitry is off when the timer is disabled. The OR Gate (U68) is used as a buffer to drive the MOSFET (Q6) in the Speaker Drive circuitry.

The master clock signal for the Timer/Counter comes from a counter (U70), which takes the output clock frequency (9.216 MHz) of the UART (U84) and divides it in half (4.608 MHz).

INTERRUPTS

The microprocessor uses four external edge-sensitive interrupt lines (INT0-3).

INT0 is tied to the HI_INT signal, which is asserted whenever an LED_HI or INAMP_HI condition exists. Refer to the FSpO2 STATUS FLAGS section below for a description of the HI_INT circuitry.

INT1 is connected to the UART's interrupt request line.

INT2 is tied to the A/D subsystem CC_INT signal, which notifies the microprocessor upon completion of an A/D conversion.

INT3 is used for monitoring the mains frequency AC_INT signal to allow the system to optimize its internal clock frequencies for operation in a 50 or 60 Hz environment.

DMA

DRQ0 (DMA channel 0 request) is not used at this time.

LATCHED DIGITAL OUTPUTS

The octal latch (U81), clocked by OUTPUT_CS*, is used to latch the following digital information (in order, MSB first):

PATTERN(2): Most significant address line used to select Pattern Generator patterns.

PATTERN(1): Address line used to select pattern.

PATTERN(0): Least significant address line used to select pattern.

TONE_GATE: Active high signal used to enable speaker driver.

WATCHDOG1: Used to reset the fail-safe watchdog timer on the Power Supply PCB. This signal is set to one state during the program main loop and set to the other state during one of the interrupt handlers.

RESTORE_BASELINE*: Not used at this time.

CH1/CH2*: Signal used to select analog inputs to be digitized by the A/D converter. Only CH1 is used at this time.

REDUCE_GAIN*: Active-low signal used to reduce the post-DAC amplification in the INAMP gain stage.

WATCHDOG

The WATCHDOG signal is used to reset the fail-safe watchdog circuitry on the Power Supply PCB. WATCHDOG1 (described above) is set to one state during the program main loop and set to the other state during one of the interrupt handlers. The signal is OR'd (U68) with LED_SHUTDOWN. During normal operation WATCHDOG (the OR gate output) toggles continuously, resetting the

watchdog circuit on the Power Supply PCB. If this signal stops toggling, the watchdog circuit times out and the Power Supply turns off power to the Processor PCB.

SERIAL COMMUNICATION

Internal communication between the Patient Isolated Section and Communication Section of the Processor PCB is accomplished through a serial communication link that is optically isolated to maintain the patient isolation required. The Communication Section serial communication circuitry is discussed in Section 5.3.3.

The Patient Isolated section uses a UART (U84) to handle the serial communication between itself and the Communication section. Communications are handled with TxD and RxD signals. TxD is inverted by the Transistor (Q5) which also provides the drive, OPTOUT*, for the Opto-coupler (U21). Transmission from the Communication section, OPTIN*, is provided through the Opto-coupler (U23). OPTIN* is inverted by the Transistor (Q19), which in turn drives the RxD input.

The UART runs off of its own 18.432 MHz crystal whose frequency is divided in half internally. The DCD* pin is programmed to output this 9.216 MHz clock externally. A circuit consisting of a transistor (Q18), resistor (R110), and capacitor (C210) is used to drive the RTS* (Request To Send) pin low during reset, configuring the UART to use the external crystal.

QUIET BUS

To minimize digital noise injection into the analog circuitry, a "quiet" analog-side data bus is provided. A transparent latch (U60) buffers the QUIET_ADDRESS and QUIET_DATA digital signals used by the analog circuitry, allowing the address and data lines on the analog side to change state only when specific analog elements are written to. These elements are comprised of the LED drive/ speaker volume DAC (U66), the INAMP DAC (U43), and the analog MUX (U28). Any other write or read cycle initiated by the microprocessor will not affect the digital bus on the analog side.

The 3 input NAND gate (U61) latches data bits 0-7 and address bits 1 and 2 whenever DAC_WR*, INAMP_CS*, or ANALOG_MUX_CS* are asserted.

The LED drive/speaker volume DAC (U66) is susceptible to output glitches due to the propagation delay of the NAND gate (U61) and transparent latch (U60). The two inverters (U71) provide adequate delay for DAC_WR*. The output of the second inverter, SIGNAL, drives the write input of the DAC.

PATTERN GENERATOR

The Pattern Generator circuitry is a finite state machine used to set up the various timing signals used by the FSpO2 circuitry. These signals control the phase and rate of the LED drives, the gain and timing of the synchronous detector, and the gating of signal energy into the low-pass analog filters.

The heart of the Pattern Generator is an EPROM (U64) capable of supporting a total of eight different timing patterns, each of which is 256 elements long.

The addresses for the EPROM are provided by an 8-bit up-counter (U76), whose count is incremented once each PG_CLK cycle; this clock normally runs at 104.727kHz. To prevent switching glitches from the EPROM from affecting the analog circuits, the output of the EPROM is buffered by an octal latch (U65). Note

that the counter is triggered by the inverted (U71) falling edge of PG_CLK, while the latch is clocked by rising edge; this gives the new information from the EPROM time to settle before being transferred into the latch.

The output latch controls the following signals (in order, MSB first):

SYNC_INVERT*: Controls the gain of the +1/–1 amplifier in the synchronous detector; a logic high causes the gain to be +1.

NOISE_GATE: Not used at this time.

SPARE_GATE: Not used at this time.

SPARE_LED*: Not used at this time.

RED_GATE: Allows signal energy from the sync detector to pass into the "RED" low-pass filter chain. This signal is active high.

RED_LED*: Activates the Red LED drive. This signal is active low.

IR_GATE: Allows signal energy to pass into the "IR" low-pass filter chain. This signal is active high.

IR_LED*: Activates the IR LED drive. This signal is active low.

STATUS INPUTS

The STATUS_RD* signal is used to put 16-bits of system status information on the microprocessor bus through a buffer (U85) for the lower byte and a latch (U58) for the upper byte. The lower byte of status information comprises the following (in order, MSB first):

N/A: Always high.

SWITCH_STDBY: High when the front panel switch is in the standby position.

N/A: Always high.

LED_LOW: High when the **SAT** input signal level is low.

W15: Low when jumper W15 installed

W14: Low when jumper W14 installed.

W16: Low when jumper W16 installed.

W17: Low when jumper W17 installed.

The upper status byte provides LED state and interrupt source information during a "**HI_INT**" condition. The **LED_HI*** and **INAMP_HI*** status flags are NANDed together (U61). When either flag is asserted (low true), the output of the NAND gate goes high. This state is synchronized to the 10 MHz microprocessor clock, **CLOCKOUT**, by the first flip-flop (U75), then delayed one clock cycle by the second flip-flop (U75). This delay is necessary to ensure set-up times are met for the status latch. The output of the second flip-flop is used to generate an interrupt to the microprocessor and to latch the following status information into the status latch (U58), in order, MSB first:

INAMP_HI*: Low when an INAMP_HI condition triggered the interrupt.

LED_HI*: Low when an LED_HI condition triggered the interrupt.

N/A Always low.

N/A Always low.

N/A Always low .

SPARE_LED*: Not used at this time.

RED_LED*: Low when the interrupt occurred during the RED LED on state.

IR_LED*: Low when the interrupt occurred during the IR LED on state.

Analog Subsystem

SPEAKER DRIVER

The Speaker Driver circuitry controls the activation, volume, and tone of the speaker. The tone frequency is provided by the external timer (U80). TONE drives the gate of a MOSFET (Q6). The drain of the MOSFET drives the lower leg of the speaker, SPEAKER(-) with a square wave of the selected frequency. The frequency selected depends on the function desired.

Channel four of the DAC (U66) is used to turn the speaker on and off, as well as set the volume. The output, VOLUME_V, drives the input circuitry of an op amp (U63). Since the speaker is driven from the +5V digital supply, but the DAC provides a 0–10 Volt output, a resistor divider (R59, R60) divides the DAC output by 2 to produce a 0–5 Volt signal. The capacitor (C156) filters this signal. The op amp output is buffered by an NPN transistor (Q7). The R-C network (R58, C154) helps shape the square wave drive into quasi-sinusoidal waveform for the speaker, producing the desired tone for the frequencies that are used.

The diode (CR21) clamps the flyback voltage created by the inductance of the speaker when Q6 turns off.

The Speaker is mounted to the chassis and is connected through the 2-pin connector (J16).

PRECISION REFERENCE

Two reference voltages are used in the Analog Subsystem. A 10.0 VDC reference and a 4.52 VDC reference which is derived from the 10.0 VDC reference.

10.0 VDC REFERENCE

The 10.0 VDC reference is derived from a REF-01 10 Volt Precision Reference (VR4). The output is filtered by a 22µf capacitor (C97). This VREF_10V reference is used by the DAC (U66), the 4.52VDC Reference (described below), and the Low Pass Filter Chains (described below).

4.52 VDC REFERENCE

The 10 Volt Reference is scaled by a resistor divider (R324, R325) to yield a nominal 4.5205 Volt signal. A 10µf capacitor (C99) helps attenuate high frequency noise from the reference. This voltage is buffered by an OP27 Operational Amplifier (U29). Note the R-C network at the output of the op amp (R381, C116, C117) and in its feedback loop (R380, C102). This forms a low-pass filter (f_c=277 Hz) which is used to further reduce high frequency noise, as well as lower the output impedance of the circuit at the Analog-to-Digital Converter (ADC) conversion frequency. The resistor (R378) provides DC feedback for the op amp.

Aside from providing a very low-noise reference for the ADC, this circuit also provides, through an op amp (U49), a buffered reference signal, BUFFERED_VREF_4.5V, for the RCAL measurement circuitry.

FSpO$_2$ CIRCUITS

The FSpO$_2$ circuitry comprises the LED Driver, the Input Filter Stage, the Programmable INAMP Gain Stage, a synchronous detector, two low pass filter chains, and associated status flags.

THE LED DRIVER

The LED intensities are set with a quad 8-bit DAC (U66), which is referenced to 10 Volts. Each LED has its own DAC output. The LED drive voltages are multiplexed via an analog switch (U54). The Pattern Generator output signals **IR_LED*** and **RED_LED*** control which LED drive voltage is gated through to the LED current driver.

The gated LED drive voltage signal is connected to an R-C filter and voltage divider (R54, C133, R329, R332) providing a 498.8mV signal to the op amp (U44) when a DAC output is set to maximum. A 499K resistor (R300) tied to –5 VA provides a small negative bias to the drive voltage, ensuring that the LED current driver is completely turned off when the DAC outputs are set to 0 VDC. A diode (CR16) provides a feedback path during this time, clamping the op-amp output to roughly –0.6 Volts. This allows the op amp to slew back quickly when it is turned on again.

The LED current driver consists of an Operational Amplifier (U44), 6 transistors (Q8, Q9, Q10, Q12, Q14, and Q15), and their associated discrete components. The two PNP transistors (Q14, Q15) act as switches, connecting the filtered (R331, C129) +5V digital supply to the anode of the LED being turned on. The active low signals, **IR_LED*** and **RED_LED***, control the states of these PNP transistors. Two NPN transistors (Q9, Q12) buffer the output of the amplifier, allowing the circuit to drive up to 84 mA of peak current through a single LED. Two additional NPN control transistors (Q8, Q10) are used to turn on and off the buffer transistors mentioned above. These transistors are also controlled by **IR_LED*** and **RED_LED***. Logic high voltages on these lines cause the corresponding control transistors to saturate, pulling the bases of the buffer transistors connected to them low and thus turning off those transistors. Conversely, a logic low voltage on one of these lines causes the corresponding control transistor to turn off, enabling the buffer transistor connected to it. Note that only one buffer transistor should be enabled at a time. Taken as a whole, these transistors form a bi-directional current source, allowing the two primary LEDs to be connected in reverse-parallel.

An Operational Amplifier (U44) regulates the LED drive current. The control voltage used to set the current through the LED is applied to the non-inverting input of the op amp. The timing signals from the Pattern Generator set up the transistors in the LED driver circuit such that current flows from the digital supply, through the LED, through one of the buffer transistors, and finally through the equivalent 5.95_ current-sense resistor (R338 and R336 in parallel) to ground. The voltage drop across this resistance is then fed back via a 1k resistor (R333) to the inverting node of the op amp. The op amp will drive the buffer transistors to force this feedback voltage to equal the input voltage. Thus, the LED current is equal to the input voltage divided by 5.95 _. Because of the relatively large current demands of the LEDs, their drive current is pulled from the digital supply

to help minimize noise on the analog supplies. The op amp compensates for voltage changes on the digital supply in order to keep the current constant.

LED OVERCURRENT PROTECTION

During normal operation, the rise in LED temperature is well below safety limits for contact with the fetus. The LED overcurrent protection circuit helps ensure that the maximum average current delivered to a LED cannot produce an unsafe temperature rise.

The voltage drop across the resistor (R331) that filters the digital +5V used to power the LED drive is filtered by a 10µf capacitor (C184) through a 2k resistor (R398). The voltage across this capacitor is compared to a voltage created by the voltage divider (R399, R400) and by a comparator (U78). If the voltage across the capacitor exceeds 89mv, the output of the comparator, LED_SHUTDOWN, goes high and inhibits WATCHDOG1 through an OR gate (U68). The OR gate output, WATCHDOG, is then held high and the watchdog circuitry on the Power Supply PCB times out and the power to the Processor PCB is shut off.

THE PASSIVE INPUT FILTER

The amplified photo current **SAT** signal from the external Patient Module contains negative pulses when the detector of the sensor receives light from the LEDs. This signal first passes through a passive high pass filter (C106, R301). The output of this circuit is then buffered with an op amp (U44) to eliminate loading effects on the filter and to provide a low impedance drive to the INAMP DAC (U43). The corner frequency is approximately 31Hz.

INAMP

Due to the very high dynamic range requirements of oximetry signals, some form of programmable gain stage is required for the photo current signal. This function is realized using an 8-bit multiplying DAC (U43) and op amp (U36) as a programmable attenuator with 255 possible settings. This programmable attenuator is followed by a two state fixed gain stage consisting of an op amp (U42) and its associated discrete components which are configured as a non-inverting amplifier. This fixed gain stage provides some low pass filtering with a corner frequency of about 16kHz, and it offers two levels of gain which are determined by the state of the switch (U52). With this switch open, the gain is set to a value of 51 by R302 and R303, and the filtering is determined by C307. With the switch closed, R341 and C324 are connected in parallel with R302 and C307 which sets the gain to a value of approximately 12.75 and maintains the same filter corner frequency.

The fixed gain is maintained at the lower gain setting when the input signal levels are high in order to reduce the system noise floor as much as possible. The higher gain setting is employed when lower signal levels require the increased gain capability. Linearity between the two fixed gain settings is maintained by shifting the programmable attenuator setting by two bits (a factor of four) in the appropriate direction. Both fixed gain settings allow the programmable attenuator to operate over its full range of 255 settings, providing a very broad range of programmable gain settings for this stage that the system can use when optimizing the signal levels.

THE SYNCHRONOUS DETECTOR

After passing through the INAMP gain stage, the signal is then synchronously

demodulated by a differential amplifier/analog switch combination and demultiplexed by two analog switches leading into the filter chain circuitry.

A Differential Amplifier (U34) and a switch (U41) form a +1/–1 gain stage. The gain is determined by the state of the SYNC_INVERT* digital signal. When SYNC_INVERT* is low, the switch connecting pins 3 and 4 of the switch closes, while the switch connecting pins 1 and 16 opens. This causes the non-inverting input of the differential amplifier to be tied to ground, turning it into an inverting amplifier with unity gain. When SYNC_INVERT* is high, the states of these switches reverse, causing the amplifier to become configured as a non-inverting unity gain amplifier.

The SYNC_INVERT* signal comes from the Pattern Generator. The timing of this signal is such that whenever an LED is turned on in the sensor, this signal will be low, and during LED off states, this signal will be high. The +1/–1 gain amplifier allows the system to reject low frequency common-mode noise riding on the photo current signal. The system measures the scaled photo current signal during times when the LEDs are turned on (measuring wanted signals plus any additive noise), and adds to these signals an inverted version of the same photo current signal measured during times when the LEDs are turned off (additive noise only). Assuming the LED on and off measurements are made close together in time and that the interferring noise is at a relatively low frequency compared to the LED strobe rate, the addition of these two signals in the low pass filter chains lead to the cancellation of the additive noise (for example, signal = [signal + noise] + [- noise]).

The output from the +1/–1 gain amplifier feeds into the demultiplexing analog switches (U40), which are used not only to demultiplex the photo current/ inverted-off-state signal energy into separate low pass filters (one for each LED signal), but also to prevent switching-spike energy from the +1/–1 gain amplifier from coupling into these filters. The control signals for these analog gates, IR_GATE, and RED_GATE, come from the Pattern Generator and are timed such that only the last portion of each signal state is actually gated into the filters insuring that only the fully settled signal plateaus are gated.

An Inverting Amplifier (U35) and an additional switch (U41), allows either the IR signal (from the +1/–1 amplifier) or an inverted version of it to be gated into the IR filter chain, depending upon the state of PATTERN(2). Under normal conditions, PATTERN(2) is low, causing the non-inverted form of the IR signal to be gated into its low pass filter.

THE LOW PASS FILTER CHAINS

After the photo current/inverted-dark-state signals have been demultiplexed by the above mentioned analog gates, they are passed into separate analog low pass filters. Each filter consists of two identical 2-pole multiple feedback filter stages (U39, U38), yielding an overall cut-off frequency of around 8 Hz. The overall gain of these filter chains is approximately 9.

After the second 2-pole filter, the signal goes to a final 1-pole inverting gain stage, with a gain of about 1.86. These gain stages provide an additional pole of filtering at 14 Hz. An offset voltage is also added to the signal at this point, ensuring that each filter chain’s output voltage will be above 0 Volts (the lower limit of the system's A/D conversion range), even with worst-case component tolerances. This offset voltage is derived from the 10 Volt Reference, **VREF_10V**, that is divided

down and filtered via the discreet components (R326, R327, C320, C121) to approximately 90mV. Since the output stage of the filter chain has a gain of 2, the resulting output voltage (if the previous stages produce 0 Volts) is equal to (90mV * 2) +90mV or a nominal 270mV.

FSpO2 STATUS FLAGS

Three flags are used to notify the microprocessor of changes in the FSpO2 signals, LEDHI*, LED_LOW, and INAMPHI*.

LEDHI* is an active low signal used to notify the microprocessor that at least one of the LED drive signals needs to be reduced. The circuit generating this signal consists of a Comparator (U78) and its associated support resistors and capacitor. A resistor divider (R91, R97) generates a stable reference voltage of approximately –10V for the comparator that is filtered by a 0.22µf capacitor (C163). The other input of the comparator monitors the output of the Patient Module, **SAT**. If this signal drops below the –10V threshold, the output of the comparator goes low. The 1M_/51.1k_ resistor combination (R92, R94) provides approximately 25mV of hysteresis for the comparator. The open collector output is pulled high by a 22.1k resistor (R96). It is assumed that this flag will only be asserted during LED on states. During such a condition, both this signal as well as the current LED on status (that is, Red or IR) are latched into the status register (U58), and a **HI_INT** interrupt to the microprocessor is generated. Upon receipt of this interrupt, the microprocessor reads the status register to determine which state caused the error condition and reduces the appropriate LED drive level.

LED_LOW is an active high signal that notifies the microprocessor that the LED drive level can safely be increased. A fast attack/slow decay negative peak detector is used to monitor the output of the Patient Module, **SAT**. The charge time constant of this circuit, set by a 1k_ resistor (R52) and 2.2µf capacitor (C130) through a diode (CR15), is approximately 2ms. The discharge time constant, set by the same 2.2µf capacitor and a 10M_ resistor (R340), is approximately 22 seconds. The output of this circuit is buffered by an op amp (U53) and feeds into a Comparator (U78) whose threshold is set at approximately –5 Volts with the discrete components (R89, R90, C162). The resistors (R87, R66) provides approximately 25mV of hysteresis for the comparator. The open collector output is pulled high by a 22.1k resistor (R88). If the output of the preamplifier remains above –5 Volts for a relatively long period of time, then the **LED_LOW** flag will be asserted, notifying the microprocessor, which polls this signal periodically, that it may safely attempt to increase the LED drive levels. The purpose of this flag is to prevent the microprocessor from continually changing the LED drive levels during periodic large amplitude changes in ambient light levels (for example, a sensor being moved in and out of direct sunlight). Note that even with the high dynamic range of the front end, this signal will almost always be asserted, even when the LED drive levels are at their maximum levels. This is particularly true in the fetal environment, where virtually no external ambient light exists.

INAMPHI* is an active low signal which notifies the microprocessor that the input amplifier gain needs to be reduced. Note that this information cannot be determined solely from the outputs of the analog filter chains, because the synchronous detector between the INAMP stage and the filter chains removes low frequency common-mode signals which may cause the INAMP stage to saturate. The output of the INAMP stage is compared to an approximate 10V threshold

(divider R93, R95, C164) by comparator (U78) and its associated circuitry (R65, R98, R99). Whenever this threshold is exceeded, the state of **INAMPHI*** is latched into the status register, and a **HI_INT** interrupt is generated. The microprocessor responds to this interrupt by reducing the INAMP gain.

RCAL MEASUREMENT

The Rcal circuit is used to measure the calibration resistor located within each sensor. This resistor forms the lower leg of a voltage divider referenced to the precision 4.52 Volt Reference voltage **BUFFERED_VREF_4.5V**. The upper leg of the divider is a precision 0.1% 7.50kΩ resistor (R360). A 0.47µf capacitor (C157) helps filter noise above about 200 Hz. The output signal is buffered by an op amp (U49). The output, **RCAL_V**, is then digitized by the A/D converter.

CONTACT MEASUREMENT

Timer 0 of the microprocessor generates a 50 kHz square wave **SENSOR UP CLK** signal which goes through a passive single-pole high-pass filter (C170, R80), followed by a 2-pole active low-pass filter with a gain of about 3.3 (U55). The resulting quasi-sinusoidal waveform has a peak-peak amplitude of approximately 10 Volts. This voltage is then AC coupled with a 0.01µf capacitor (C136) and used to drive the primary of a signal transformer (T1) via a 100k_ resistor (R56), which limits the current in the transformer primary to a maximum of 100µA peak-peak.

The secondary of the transformer is connected across the contact pins in the sensor via two series 0.01µf capacitors (C166, C187) which prevent DC currents from flowing in the transformer secondary. A current of approximately 95µA is coupled into the transformer secondary and flows through the impedance between the contact pins, generating a voltage. This voltage is then reflected back to the primary of the transformer and amplified by a voltage gain stage (U55, R72, R75) of about 5.5. The signal positive peaks are then detected by a diode (CR24), 1k_ resistor (R73), and 0.1µf capacitor (C169) and held by the same 0.1µf capacitor working against the 1M_ bleed resistor (R78). The values selected allow the peak detector circuit to follow signals on the order of 1Hz.

The signal is then buffered with an op amp (U35) and becomes the **SENSOR_UP** input signal to the analog multiplexer. This voltage is digitized by the system A/D converter and compared against software contact thresholds.

ADC CIRCUITS

The microprocessor analog-to-digital subsystem comprises a 2-channel 16-bit Analog-to-Digital Converter (ADC), an 8-input analog multiplexer, and a microprocessor interface unit.

THE A/D CONVERTER

The heart of the A/D subsystem is a 16-bit successive approximation Analog-to-Digital Converter, or ADC (U46). The ADC is a two-channel device. Only one channel may be digitized at a time. The system selects the appropriate channel to digitize using the **CH1/CH2*** signal, which is one of the latched output bits in the digital subsystem. Only Channel 1 is used at this time. Conversions are initiated by the microprocessor by activating the PCS1 chip select line (labeled **ADC_START***). The ADC clock is generated by a binary counter (U70) which takes the 9.216 MHz clock generated by the UART (U84) and divides it by 8 to yield a 1.152 MHz clock signal called **ADC_CLK**.

The power supplies to the ADC are passively de-coupled and filtered. The analog ±5VA supplies are generated by linear regulators (VR6, VR5) on board the Processor PCB, then filtered by 100µH inductors (L5, L4) and 2.2µf capacitors (C114, C113), paralleled by 0.1µf capacitors (C109, C336) for better high frequency rejection. Due to the fairly stringent power supply requirements of the ADC, the digital ±5 Volt supplies come off of the analog ±5 Volt supplies, buffered via 10_ resistors (R387, R386) and further de-coupled with 2.2 µf/0.1µf capacitor networks (C333, C110, and C335, C112).

The ADC has separate analog and digital grounds, which are tied to the respective ground planes on the PCB. A jumper (W7) allows these two planes to by tied together at the ADC. The present design leaves this jumper open.

THE ANALOG MULTIPLEXER

The A/D system uses an 8-to-1 analog multiplexer (U28). This MUX has the following input signals:

IR_V: The filtered IR signal from the FSpO2 circuitry.

RED_V: The filtered red signal from the FSpO2 circuitry.

NOISE_V: Not used at this time.

SPARE_V: Not used at this time.

SENSOR_UP: The sensor contact voltage generated by the impedance between the sensor contact pins.

RCAL_V: The signal generated by the Rcal measurement circuit.

POWER_V: The voltage from the power supply PCB used to determine whether the instrument is operating off of the correct AC mains supply.

DISPLAY_V: The signal from the display PCB used to determined LED segment current.

The microprocessor selects the appropriate signals to gate through the MUX using the **QUIET_DATA** bus and the **ANALOG_MUX_CS*** signal. The **QUIET_DATA** bus is byte-wide. When accessing the MUX, the lower nibble is used to choose the appropriate input signal in the MUX. The most significant bit of this lower nibble enables the MUX output (the output enable function is active high), while the lower three bits contain the binary information of the channel to select (1-8). The upper nibble is not used at this time.

The MUX output is buffered from the ADC input with two 100 _ resistors/ 0.001µf capacitor R-C network with clamping diodes (R384, R383, C332, CR9, CR10). These provide some high frequency filtering and help reduce the effects of charge transients on the signal being digitized during conversions. The clamp diodes protect the input of the ADC from transients that may exceed the input specifications of the converter.

BUS INTERFACE UNIT

The ADC is configured to provide a self-clocked serial output stream. In order for the microprocessor to read the results of the A/D conversions with little overhead, this serial data must be converted into a digital word.

The output data is clocked by the ADC at the end of the conversion. This clock signal, SCLK, is used to clock a 4-bit counter (U56), a flip-flop (U45), and two

shift registers (U57, U59). As each bit is clocked out of the ADC, it is shifted into the 16-bit serial-to-parallel converter formed by the two shift registers. At the same time, the counter is incremented. When 15 bits have been transferred, the RIPPLE CARRY output of the counter becomes active high. When the 16th clock pulse is generated, causing the final bit of the conversion to be shifted into the shift register, the active state of the RIPPLE CARRY line causes the flip-flop to become set. This action generates the **CC_INT** interrupt to the microprocessor and causes the data held in the two shift registers to be transferred to their respective output latches. When the microprocessor reads this data, **ADC_READ*** goes low, resetting the counter and the flip-flop.

Finally, note that when the microprocessor starts an A/D conversion by bringing **ADC_START*** low, the two shift registers are cleared. This ensures that framing errors will not occur.

Processor PCB - Communications Section

The Communication Section contains the electronics for communicating with, and monitoring signals to and from, the outside world. It monitors the configuration and control switches, controls communications to the outside world (printer or computer), controls the analog input and outputs, and communicates with the Patient Isolated section.

AC power for this section is provided by the Power Supply PCB through a 2-pin connector (J6). Communications to the outside world is provided through a 9-pin subminiature “D” connector (J14) for RS232 communications. Two analog outputs, FSpO2 (J10) and PLETH (J11), are provided through 0.097-inch subminiature phone jacks. An ECG input is provided through a 0.097-inch subminiature phone jack (J13). Serial communications to the Patient Isolated section are through two opto-isolators (U21, U23).

Note: The PLETH waveform analog output is not intended for any diagnostic purpose.

The section is powered from a separate winding in the power transformer through a 2 pin connector (J6). This AC input is typically 7.5Vrms. The AC input is rectified by a Full Wave Bridge Rectifier (U18) and then filtered with a 10,000µf capacitor (C94) creating an unregulated DC voltage of approximately 9.2VDC.

The 9.2VDC is regulated by a 5 Volt linear regulator (VR1). The PNP transistor (Q1) provides a current boost. The fuse (F1) provides overcurrent protection. The 220µf capacitor (C75) filters the +5 Volt output of the regulator (+5VC).

The ±15VDC is provided by a Charge Pump Regulator (VR3). The outputs of this regulator (+15VC and -15VC) are filtered by 68µf Capacitors (C92 and C93).

The ground plane for this section is separate from the Patient Isolated section. This ground is common for both the analog and digital circuits in this section.

Digital Subsystem

MICROPROCESSOR

The Communications Section of the Processor PCB uses a microprocessor (U7) with a 6.144MHz crystal (Y1), yielding a bus rate of 3.072MHz.

RESET

The RSTIN* signal to the microprocessor is generated by a watchdog IC (U19). This IC monitors power, controls power on reset, and provides a watchdog function.

The watchdog RST* output becomes an active low if +5VC falls below 4.5 Volts. RST* remains low until power is restored. When power rises above 4.5 Volts, RST* stays low for 250ms to allow the power supply and microprocessor to stabilize. This feature is also used for the power on reset function.

The IC monitors the SOD output pin of the microprocessor. If SOD does not provide a high to low transition in 1.2 seconds, the RST* output becomes an active low for a minimum of 250ms, resetting the microprocessor. A 4.99k resistor (R29) is provided because the output of the watchdog is an open collector.

The RSTOUT microprocessor output signal is used to reset the two UARTs (U11 and U22).

ADDRESS LATCH

The microprocessor multiplexes the lower byte of the address with data. An octal latch (U1) latches the current lower byte address onto the address bus, **C_A<15..0>**, when ALE is asserted from the microprocessor.

MEMORY

The Communications section uses a PROM (U20) for program memory. Address input A14 is tied to ground via a trace at jumper W6. This allows only the first half of the PROM to be used for a total code space of 16K bytes.

The section also uses an 8k x 8 static RAM (U8).

CHIP SELECTS

The **C_IO/M*** signal from the microprocessor enables external address decoders that are used to generate chip selects as described below. All chip selects are memory mapped.

The chip selects are generated by two address decoders whose outputs are enabled only when **C_IO/M*** is asserted low. The first address decoder (U3) controls the chip selects for memory (**C_ROM*, C_RAM***). At address 8000H, the second address decoder (U10) is selected by the first decoder. All I/O function chip selects are memory mapped starting at this address. These decoded outputs are, in order from lower to higher addresses:

C_DAC*: Selects the FSpO2 / Pleth DAC (U12).

External Timer: Selects the external timer (U4).

Multiplexer Select: Selects the Analog Multiplexer (MUX) chip (U14) during a write cycle. This chip select is OR'd (U9) with **C_WR*.** When both inputs are low, the output, **C_MUX***, is asserted.

Status Select: Selects the Status Buffer (U2) during a read cycle. This chip select is OR'd (U9) with **C_RD***. When both inputs are low, the output, **C_STATUS***, is asserted.

User Configuration Select: Selects the User Configuration buffer (U5) during a read cycle. This chip select is OR'd (U9) with **C_RD***. When both inputs are low, the state of the User Configuration Switch (SW3) is read.

External UART Select: Selects the UART (U11) that communicates to the outside world.

Internal UART Select: Selects the UART (U22) that communicates to the Patient Isolated Section.

TIMER

The Communications Section contains one timer (U4). Timer 0 generates the real-time interrupt **C_RST7.5**. Timers 1 and 2 generate the BAUD clocks for the Internal and External UARTs, respectively. The timer is driven by the microprocessor clock, **C_CLK**.

INTERRUPTS

The microprocessor uses three external interrupt lines (RST5.5, RST6.5, and RST7.5).

C_RST7.5 is tied to the timer (U4) discussed above. This interrupt is rising edge latched.

C_RST6.5 is connected to the Internal UART RxRDY line. This interrupt is high level sensitive and must remain high until acknowledged.

C_RST5.5 is connected to the External UART RxRDY line. This interrupt is high level sensitive and must remain high until acknowledged.

SERIAL COMMUNICATION

The Communication section uses two UARTs to handle the serial communication between itself and the Patient Isolated section, and for external communications with the outside world.

INTERNAL COMMUNICATIONS

Internal communication between the Communication section and Patient Isolated section is accomplished through a serial communication link that is optically isolated to maintain the patient isolation required.

The UART (U22) handles communications between itself and the Patient Isolated Section. It derives the baud rate clock from the Timer 1 output of the timer (U4).

Communications are handled with TxD and RxD signals. TxD is inverted by an NPN transistor (Q4). The transistor also provides the drive, **C_FOOUT***, for the opto-coupler (U23). Transmission from the Patient Isolated Section, **C_FOIN***, is output from the opto-coupler (U21) and inverted by an NPN transistor (Q3), which in turn drives the RxD input.

EXTERNAL COMMUNICATIONS

The UART (U11) handles communications between itself and the outside world (printer, computer, electronic fetal monitor, etc.). It derives the baud rate clock from the Timer 2 output of the timer (U4).

Communications are handled with TxD and RxD signals. A combination level translator/charge pump circuit (U6) and the associated circuitry (C1, C2, C27-30, CR1, CR2) provides translation between RS232 signal levels (±10 VDC) and digital signal levels. The RS232 signals are output through the 9-pin subminiature "D" connector (J14). All I/O through this connector are filtered with an L-C network (L1, C31, C32, C34, C36, C37, C38, C39).

USER CONFIGURATION SWITCHES

The10-position rear-panel dip switch (SW3) is used to configure communications format (positions 6-8), baud rate (positions 3 and 4), and analog output range (position 1). Positions 2, 5, 9, and 10 are not used at this time. Refer to the operator's manual for the various configurations. Switch positions 3–10 are tied to ground on one side and pulled up with one element of a 100k resistor pack (RP2). The 10k resistor packs (RP3, RP4) provide ESD protection for the buffer (U5).

Switch position 1 is tied to ground on one side and **C_SCALE** on the other. Closing the switch grounds one side of the precision resistor divider (R19) which divides the output of the DAC (U12) by 10.

Analog Subsystem

ANALOG OUTPUT CONTROL AND JUMPER STATUS

The **C_STATUS*** chip select controls an 8 bit buffer (U2) for reading ZERO and FULL Scale rear-panel push button switches (SW1, SW2), configuration jumpers (W1-5) and ECG trigger (**C_ECGTRIG**). A 47k resistor pack (RP1) provides pullups for the signals. The10k resistors (R1-4) protect the push button switch inputs of the buffer from ESD spikes.

ANALOG OUTPUTS

DAC AND REFERENCE

An adjustable negative regulator (VR2) and associated discrete components (R33, R34, C82) provide a reference voltage of –9.98VDC, ±4%. This reference is provided to an 8-bit DAC (U12) configured as a programmable attenuator. An op amp (U13) inverts the DAC attenuated reference voltage to a positive 0–10VDC signal output. A 2k potentiometer (R16) is used to trim the Full Scale voltage output to 10.0VDC when the DAC is set to 0FFH.

SCALING

The output of the circuitry described above is fed through a precision 10:1 divider (R19). If the 10-position DIP switch (SW3) position 1 is closed, the input into the 1:8 MUX (U14) is 0-1VDC. If the switch is open, the input into the MUX is 0–10VDC.

DE-MULTIPLEXER

The MUX is controlled by the chip select, **C_MUX**, and address lines 0-2. The $FSpO_2$ output is at the first C_MUX address. The PLETH WAVEFORM output is at the second C_MUX address.

SAMPLE AND HOLD CIRCUIT

There are two identical Sample and Hold Circuits, $FSpO_2$ and PLETH WAVEFORM. The $FSpO_2$ Sample and Hold is described here. The PLETH WAVEFORM Sample and Hold theory of operation is the same.

To output the correct voltage to $FSpO_2$, the program writes the output voltage to the DAC. It then selects channel 1 of the MUX to output the voltage to the storage

capacitor (C68). The charge of the capacitor is buffered through an op amp (U15). A zener diode (CR3) protects the op amp output from external transients. The 1K resistor (R6) quells oscillations which may occur when driving high capacitive loads. The ferrite bead (FB3), L-C network (L2, C44) and spark gap (SG1) provide protection from ESD and snubs EMI transmissions.

ECG

The ECG input is filtered for EMI and ESD by the L-R network (L3, R10), spark gap (SG1) and the ferrite bead (FB2). The output of the filter is diode clamped (CR5, CR6) for input protection. The R-C network (R9, C40, C41, R25) make up a band pass filter with a lower corner frequency of 10.20 Hz and a higher corner frequency of 72.34 Hz.

Incoming ECG signals are coupled thourgh to two parallel circuits:

- •unity-gain buffer U17
- •a peak follower circuit (composed of U17, Q2, C73, R26, and R24) with slow decay that stores the peak value of the R-wave from one peak to the next.

The peak follower circuit provides an adjustable threshold for sensing each ECG R-wave peak. Voltage comparator U16 produces a positive voltage pulse (**C_ECGTRIG**) when the ECG input signal exceeds the adjustable threshold determined by previous peak R-wave values.

Display PCB

The Display PCB provides visual output to the user. Six digits provide SAT and Pulse Rate (3 each). Two 10-segment bargraphs provide pulse amplitude and signal quality information. Other enunciators provide information on ECG, Alarm, Mode, Pulse Search, Sensor Unplugged, and Sensor Lifted. The Display PCB also provides interfacing for the Front Panel Buttons (4) and Control Knob.

Connections

The +5V power is provided from the Power Supply PCB through a 2-pin connector (P4). Processor PCB signals are provided through a 14-pin dual in-line flat cable connector (P8). The Control Knob is connected through a 5-pin connector (J16).

Power Conditioning

The +5V power and ground for the circuitry is provided from the Power Supply PCB. It is filtered at the input connector (P4) by a 22µf capacitor (C10). The 0.047µf bypass capacitors (C1, C3-9, C11) filter the ICs locally.

Display Clear

The display is cleared at power on and may be cleared by the Processor PCB at any time. Power On reset is controlled by an R-C network (R2, C2, CR1) that clears a quad flip-flop (U3). Bit 3 of this flip-flop is set low by this reset, which in turn clears the three octal latches (U4, U9, U10) and disables the decoder used for energizing digits or bargraphs (U6). The microprocessor may clear the display by writing a zero (0) at any time to bit 3 of the quad flip-flop.

Addressing

Addressing is controlled by an address decoder (U1). The decoder is selected by the signal, **DISPLAY***, from the Processor PCB. These decoded outputs are as follows, in order from lower to higher addresses (0 thru 7):

0 *SEGMENT DISPLAY SELECT*: Writes the lower nibble to a quad latch (U3). Bits 0–2 drive a decoder to select a particular 7-segment digit or 10-segment bargraph display to energize. Only one digit or bargraph can be energized at a time. Bit 3 (low true) resets and clears the display. The microprocessor multiplexes this address every 2.5ms to turn on one digit or bargraph at a time to conserve power and extend display life.

1 *LOWER SEGMENTS* (A-G, DECPT): Writes to an 8-bit latch (U9) to energize segments A through G (Bits 0-6), and the segment DECPT (decimal point) (Bit 7).

2 ‘ *UPPER SEGMENTS* (H, I), and *LIGHTBARS* (SENLIFT, ECGREQ): Writes to an 8-bit latch (U10) to energize segments H and I (Bits 0-1). These two segments, along with segments A-G and DECPT, are used for the 10-segment analog displays (Pulse Amplitude and Signal Quality). The next two bits (Bits 2-3) energize the two halves of the Sensor Lifted lightbar. Bit 4 energizes the upper half of the ECG Required lightbar. Bits 5–7 are unused and do not need to be masked.

3 *LIGHTBAR SELECT:* Writes to an 8-bit latch (U4) to energize the lower half of the ECG Required lightbar (Bit 0), two halves of the Sensor Unplugged lightbar (Bits 1, 2), Mode2 lightbar (Bit 3), Searching lightbar (Bit 4), Audio Alarm Off Lightbar (Bit 5), and the two halves of the ECG In Use (labeled ECG Not In Use on the schematic) lightbar (Bits 6, 7).

4 *CONTROL KNOB COUNTER CLEAR:* A read or write to this location clears the 4-bit output of a binary counter (U11).

5 *FRONT PANEL CONTROLS SELECT:* Reads an 8-bit buffer (U12), which outputs the Button and Control Knob counter status.

6 Not Used.

7 Not Used.

Display Drivers

A total of 8 LED displays comprise the Digit and Bargraph displays (DIGIT 0 through DIGIT 5, CONF (Signal Quality), and BLIP). These displays are multiplexed (energized one at a time) every 2.5ms by the Processor PCB in order to conserve power and extend LED life. The multiplexing is software controlled.

There are also lightbars used for signifying modes and status. These lightbars are latched and only need to be updated as needed.

DIGIT AND BARGRAPH DRIVES

A quad flip-flop (U3) and decoder (U6) are used to select a particular display (1 of 8) to energize. Each decoder output (low true) drives a PNP transistor (Q1-8) through 220_ resistor packs (RP2, RP3). The transistors act as switches to select a particular display by pulling the common anode pin of that display to +5V.

The drives for the 10 segments (A through G, DECPT, H, I) of the multiplexed displays are common for each segment. Two 8-bit latches (U9, Bits 0 and 1 of U10) select the particular segments to light (high true). Each segment is driven by an output from a NPN Darlington transistor array IC (U7, 3 bits of U8) through 56_ current limiting resistor packs (RP7, RP8, RP11). The common emitter pin (GND) of these transistor arrays are tied to ground through a 1_ resistor (R1) to allow current sensing discussed below.

LIGHTBAR DRIVES

The lightbars used on the Display PCB contain either 4 or 8 individual LEDs, depending on their size. Each LED in a lightbar has its own anode and cathode pins. Each transistor in the transistor arrays drive a maximum of 4 LEDs. For lightbars that contain 8 LEDs, two transistors are used to energize the lightbar, each driving 4 LEDs.

Two latches (U4, Bits 2-4 of U10) select the particular light bars to light (high true). Each lightbar is driven by one or two outputs from a NPN Darlington transistor array IC (U5, 4 bits of U8). The common emitter pin (GND) of these transistor arrays is tied to ground through a 1_ resistor (R1) to allow current sensing discussed below.

The transistor array outputs pull the cathodes of 4 LEDs in a lightbar low. The anode of each LED is tied to it's own 100_ current limiting resistor in resistor packs (RP1, RP4, RP9, RP10, RP12) or discrete resistors (R3, R4, R8, R9).

CURRENT SENSE CIRCUIT

The LED displays may fail during the life of the product (due to heat, overcurrent, infant mortality, age, etc.). The failure mode is typically an open circuit, but may also be a short circuit. The Processor PCB can monitor whether a particular display is open or shorted by measuring the current flow through a particular display.

All of the darlington transistor array GND pins (common emitter) are tied to ground through a 1_ resistor (R1). Current flowing through an LED flows through this resistor creating a voltage across it. A non-inverting op amp (U2) amplifies this voltage by a factor of 10, and outputs it (**DISPLAY V**) to the Processor PCB A/D converter circuitry.

Due to tolerances of LED forward voltages, transistor saturation voltage, and current limiting resistors, an averaging scheme is employed to check each LED for functionality. At power up, the software first turns on all segments and reads the **DISPLAY V** voltage. It then divides this value by the number of segments energized and sets up a guard band around this value. It then turns each segment on and off, one at a time, and reads the **DISPLAY V** voltage. It then compares the results with the guard band values, insuring proper operation for each lightbar or display segment.

Front Panel Controls

The Processor PCB must monitor the Front Panel Controls for button activation or Control Knob rotation. A buffer (U12) is provided to read the Control Knob counter (U11) or Buttons 1 through 4.

CONTROL KNOB

The Control Knob consists of a two channel optical chopper, with the two channels arranged mechanically 90 degrees out of phase to each other, and a dual channel optical slot detector. A 5-pin connector provides +5V and ground to the Control Knob and inputs the two channels (**CHANNEL A**, **CHANNEL B**) from it. Each channel is fed through a Schmitt trigger inverter (U13) to debounce and square up the outputs from the knob.

CHANNEL A provides the clocking pulses for an Up/Down counter (U11). CHANNEL B provides the direction U/D signal. The phase relation between the two channels provides an UP or DOWN count command to the counter, depending on which way the knob is turned (Clockwise rotation results in count-up commands). The upper 3 bits of the knob (twos-compliment) are fed into the lower 3 bits of the buffer (U12). The pre-load inputs of the counter are tied to ground. The LD pin can be asserted by the Processor PCB to pre-load the inputs, clearing the counter.

To detect a change in the U/D counter, the Processor PCB reads the twos-compliment value of the counter output and adds it to, or subtracts it from, the software accumulated turns count. After it accumulates the counter value, the Processor PCB generates a signal to the LD line of the counter to clear it for the next count value.

BUTTONS

The four button switches, Response Time (SW1), ECG Display Button (SW2 - **D/D** on the schematic), Low Saturation Limit (SW3), and Audio Alarm Off (SW4); are tied to ground on one side. The other side of each switch is pulled up by a 47k resistor pack (RP6) and fed through a 10k resistor pack (RP5) for ESD protection. The far side of each resistor pack resistor, **BUTTON1-4** are input into bits 3, 4, 5, and 7 of the buffer (U12). Bit 6 of this buffer is set high and not used (**SPARE**).

Power Supply PCB

The Power Supply PCB provides power to the Display and Processor PCBs. It contains two switching power supplies in flyback converter configurations. The supplies are capable of providing +5V at 2 Amps and ±18V at 100ma each. A micro-power +5V supply is also incorporated for on board control logic.

The Power Supply PCB also provides On/Standby and watchdog operation. The Power Supply PCB is capable of charging and operating on a lead/acid 6 Volt battery. The circuitry is not used at this time and there is no battery in the N-400.

Connections

AC input power from the transformer is provided through a 4-pin connector (J5). The Front Panel On/Standby switch is connected through a 3-pin connector (J2). Power Supply control signals from the Processor PCB are provided through a 10-pin dual in-line flat cable connector (J1). Power to the Processor PCB is provided through a 5-pin connector (J3) and power to the Display PCB is provided through a 2-pin connector (J4).

Grounds

The power supply control circuitry is tied to power supply ground (**PGND**). The analog and digital grounds are not tied directly to this point. They are tied to a MOSFET transistor (Q3) that controls the On/Standby status of the supplies (discussed in the On/Standby Control Circuitry Section below).

Switching Supplies

A Full Wave bridge (U1) rectifies the 9.2 VAC input power from the transformer. A 18,000µf capacitor (C18) filters the output of the rectifier creating an unregulated 12 VDC, **VPS**. A three-terminal 5 Volt regulator (VR2) provides power, **+5S**, to the Pulse Width Modulator (PWM) circuitry.

The PWM (VR4) controls the +5V supply. A second PWM (VR3) controls the ±18V supply. The PWMs sense their output voltages through their inverting pin, INV and compare it to their non-inverting pin, NI, which is a divided voltage from **+5S**. The PWMs control their pulse width outputs, COLA, COLB, which drive the Schmitt trigger inverters (U6). The inverters are used to square up the output pulses from the PWMs and provide low impedance active current outputs to drive the capacitive gates of the MOSFET transistors (Q4, Q5), minimizing drain rise and fall times. Pull up resistors (R27, R41) are needed because the outputs of the PWMs are open collectors. Current sense resistors (R29, R42) provide for sensing current through the MOSFETs to insure that the transformers (T1, T2) do not saturate. The two snubbing circuits (R28, C12, and R39, C16) reduce the inductive spike created by the transformers when their respective MOSFETs turn off.

The PWMs oscillation frequency is set by the resistors (R23, R37) and capacitors (C26, C30) that are tied to the RT and CT inputs. The two PWM oscillator outputs, OSCOUT, are tied together in a master/slave configuration with the +5V PWM being the master and operating at a frequency of approximately 1/(RT . CT)

or 38 kHz. The RT/CT components of the second PWM are selected so that the calculated frequency is 10% slower than the master. This allows the master to set the frequency of the slave to the same frequency and phase as the master.

Flyback transformers (T1 T2) provide current pulses through Schottky diodes (CR11, CR12, CR14) charging the output filter capacitors (C8, C10, C11, C13). The +5V and +18V output voltages are fed back to the inverting inputs of their respective PWMs. If the voltages exceed their programmed levels set by the resistor dividers (R25, R26, and R35, R43), the outputs of the PWMs reduce their pulse width, decreasing current transfer across the transformers. If the voltages drop below their programmed levels, the outputs of the PWMs increase their pulse width, increasing current transfer across the transformers.

Ferrite beads (FB1, FB2, FB3) limit switching spikes on the output. A 6 Volt zener overvoltage transient suppresser (CR5) protects logic circuits in the N-400 from transient spikes and over voltage conditions on the +5V supply.

On/Standby Control Circuitry

The Front Panel Switch of the N-400 does not, in effect, turn power on and off. The switch is an On/Standby switch. AC power control is provided by the rear-panel power switch.

The On/Standby switch provides a momentary control (through on board logic) to start up the switching supplies when placed in the ON state. The Processor PCB enables the watchdog signal, which is fed to the on board logic on the Power Supply PCB, thus maintaining power. The switch also alerts the Processor PCB that it has been turned to STANDBY state. Once alerted, the microprocessor executes a shutdown procedure, and when completed, disables the watchdog signal.

The on board logic on the Power Supply PCB controls the state of the power supply. Note that when the switch is in the STANDBY state, power is still present in the Communications Section of the Processor PCB, as well as in the control circuitry of the Power Supply PCB.

The various states discussed below explain the operation of the circuitry.

On/Standby operation can be bypassed for debugging purposes by shorting the jumper (W1). It should be noted that the microprocessor still reacts to the On/Standby switch being placed in the On or Standby positions and even though the displays may be turned off, power is still present on the Processor PCB.

STANDBY STATE

When power is turned on to the N-400 via the rear-panel switch, a micropower low dropout regulator (U3) provides power (+5VB) to the on board logic. No watchdog signal is present so the output of the NAND gate (U4 pin 3) is high. The ON side of the On/Standby switch is disconnected so the output of the NAND gate is also high. The two NAND gate outputs cannot discharge the timing capacitor (C5). The resistor (R8) begins charging the timing capacitor. When it reaches a logic high state, the NAND gate output (U4 pin 8) resets the flip-flop (U5) which turns the MOSFET transistor(Q3) off. The switching supplies have no ground reference at this point and power and ground (digital and analog) float to approximately VPS, which is ground referenced through the filter capacitor (C18)

to PGND. At power up, the state of the flip-flop is undetermined. If the output is low at power up, the MOSFET is turned off immediately.

STANDBY TO ON TRANSITION

While in the STANDBY state, VPS voltage charges a capacitor (C1) through the Standby position of the On/Standby Switch. Positioning the switch to the ON state dumps the charge in the capacitor across the resistor (R17). The diode (CR7) limits the voltage at this point to protect the input of the NAND gate. The charge in the capacitor is quickly bled off by the resistor to ground, but while the voltage is at a logic high state, the output of the NAND gate inverts the logic level, presetting the flip-flop (U5) and discharging the timing capacitor (C5) through the diode (CR8).

Once the flip-flop output has been set, and while the timing capacitor is charging, the logic level high of the output turns on the MOSFET (Q3) and power is provided to the Processor PCB. The Processor PCB enables WATCHDOG, whose pulses are capacitively coupled (C19) to the input of the NAND gate (U4 pins 1 and 2). The diode (CR10) clamps the capacitively coupled signal to logic levels. The pulses pass through the NAND gate and periodically discharge the timing capacitor (C5) through the diode (CR9). The discharged timing capacitor keeps the output of the NAND gate (U4 pin 8) high so that the flip-flop remains set and power is maintained. During this time the capacitor (C1) discharges through the resistor (R1), keeping SWITCH_STDBY low.

ON TO STANDBY TRANSITION

When the switch is set to the STANDBY position, VPS charges the capacitor (C1) through the resistor (R14). SWITCH_STDBY goes high and the Processor PCB starts power down housekeeping (turn off displays, store data in non-volatile RAM, etc.). When completed, the Processor PCB executes an infinite loop routine that does not include watchdog pulses. The capacitor (C19) discharges (or charges if WATCHDOG is high) through the resistor (R21). The result is a logic low at the input to the NAND gate (U4). The output of the NAND gate goes high, allowing the timing capacitor to charge. When it reaches a logic high state, the NAND gate output (U4 pin 8) resets the flip-flop (U5) which turns off the MOSFET (Q3), and places the N-400 in the Standby state.

POWER ON TIME DELAY

A time delay (fast turn off/slow turn on) is provided by discrete components (CR13, R20, C9) between the flip-flop (U5) and the MOSFET (Q3) to allow the switching supplies to return to ground potential on occasions when the switch is cycled rapidly. Without this delay, cycling the switch from ON to STANDBY and back to ON might not allow the switching supplies to fall far enough to generate a reliable Power On Reset pulse to the microprocessor.

Control Power Circuitry

The Power Supply PCB is capable of operating on a 6 Volt lead/acid battery. On board circuitry can charge the battery. The N-400 does not use a battery, but the output of this circuitry powers a programmable micropower voltage regulator which, in turn, powers all of the circuitry for controlling the On/Standby function.

AC power , VCB+ and VCB- (12.5Vrms), is taken from one of the transformer secondary windings. It is rectified through a Full Wave Bridge (U2) and filtered by a 2200uF capacitor (C7) to provide a positive unregulated voltage for a three

terminal adjustable regulator (VR1). The resistor divider (R13, R11, R9) sets the voltage output of the regulator. The potentiometer (R9) allows adjustment of the voltage to set TP2 to 7.2VDC.

The current sense circuitry (R3, Q2, R12, Q1) provides overcurrent protection. Q2 turns on if the current across R3 exceeds approximately 450ma. When Q2 turns on, it pulls up the base of Q1, forcing the output of the regulator to approximately 1.30 Volts.

The programmable micropower regulator (U3) provides +5 Volts, **+5VB**, to the control components. Total current drain for the control circuits and the regulator is approximately 40µa.

Schematic, Part Locator, and Block Diagrams

The following N-400 schematic, part locator, and block diagrams are included on the foldout pages at the end of this section:

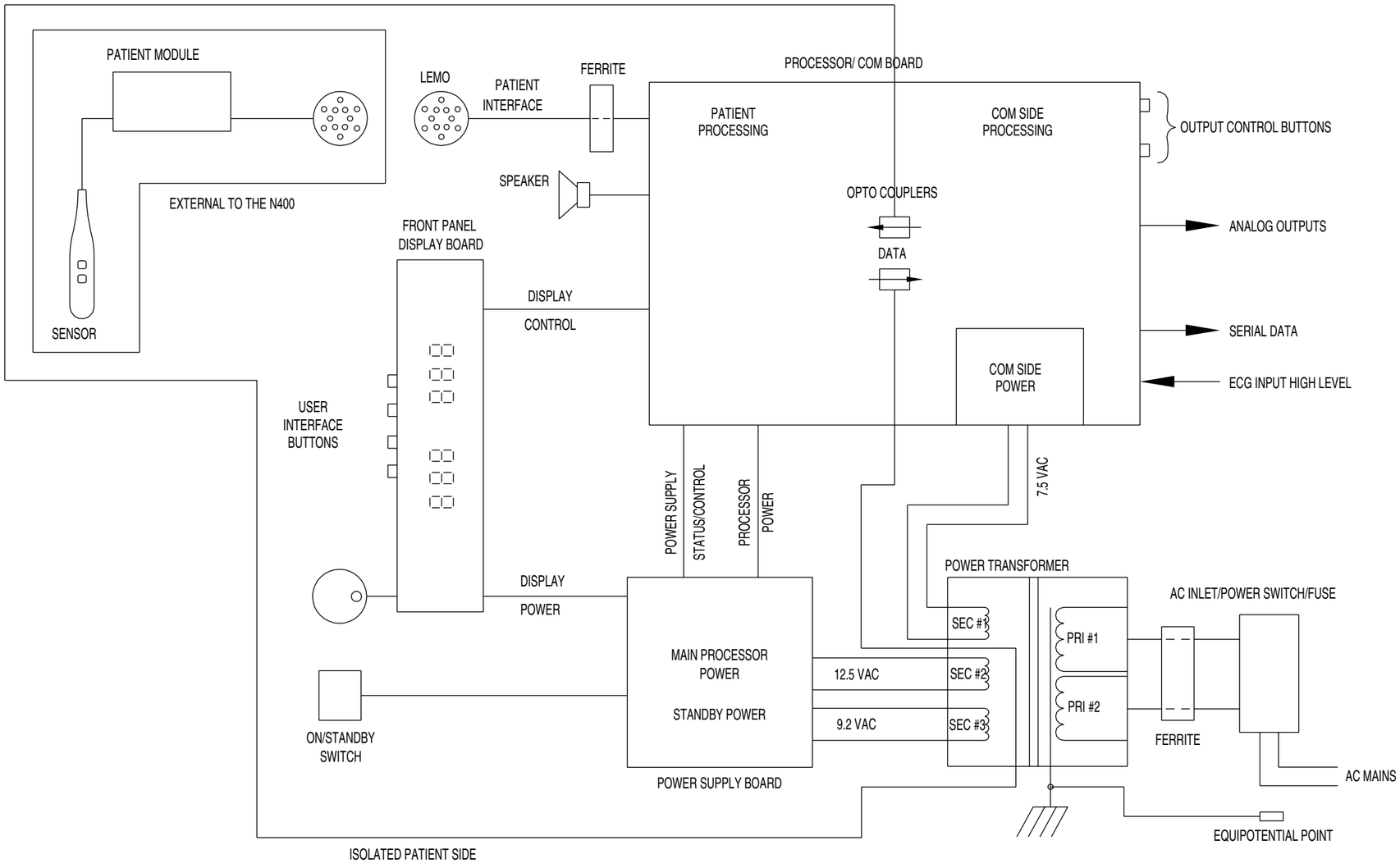
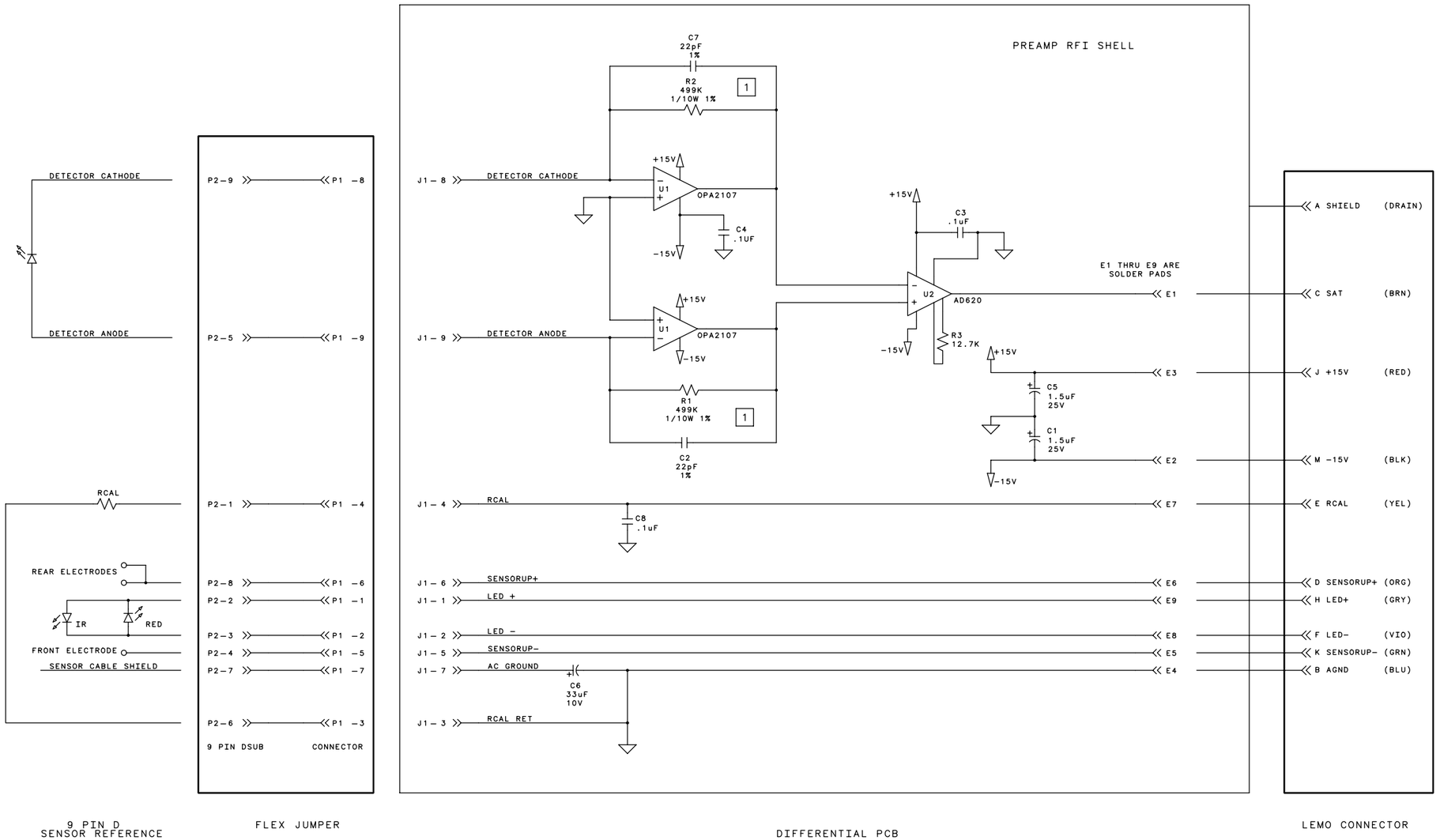


Figure 2
Block Diagram

024840



NOTES:

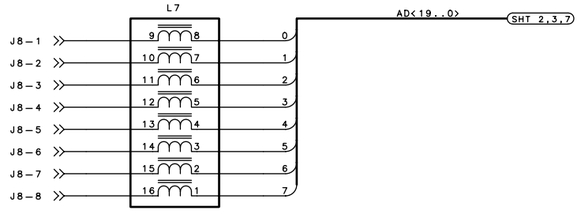
1 RESISTORS, R1 AND R2, ARE MATCHED WITHIN .02%

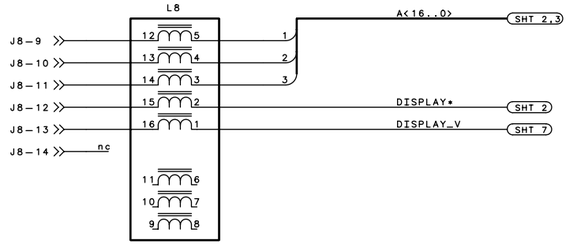
DIFFERENTIAL PATIENT MODULE INTERCONNECT

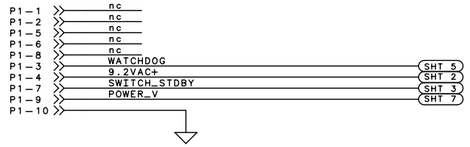
Figure 3
Patient Module Schematic and Interconnect Diagram

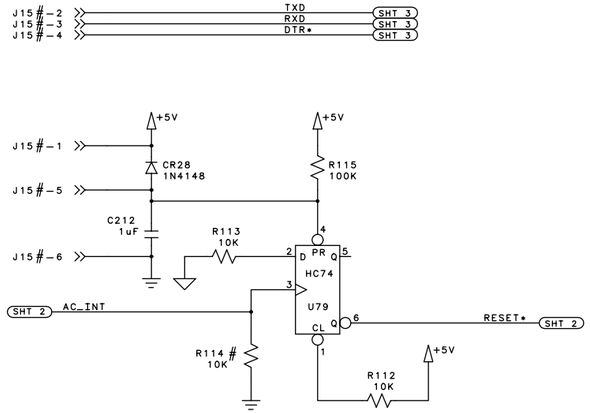
042642

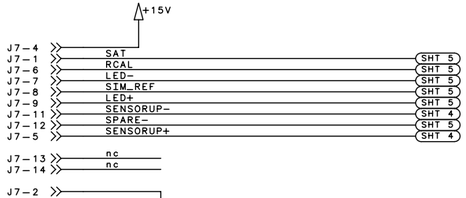
#NOTE:
J15 NOT INSTALLED ON PCBA.











POWER AND GND TABLE FOR ICS WHOSE POWER CONNECTIONS ARE NOT EXPLICITY SHOWN ON THE SCHEMATIC.

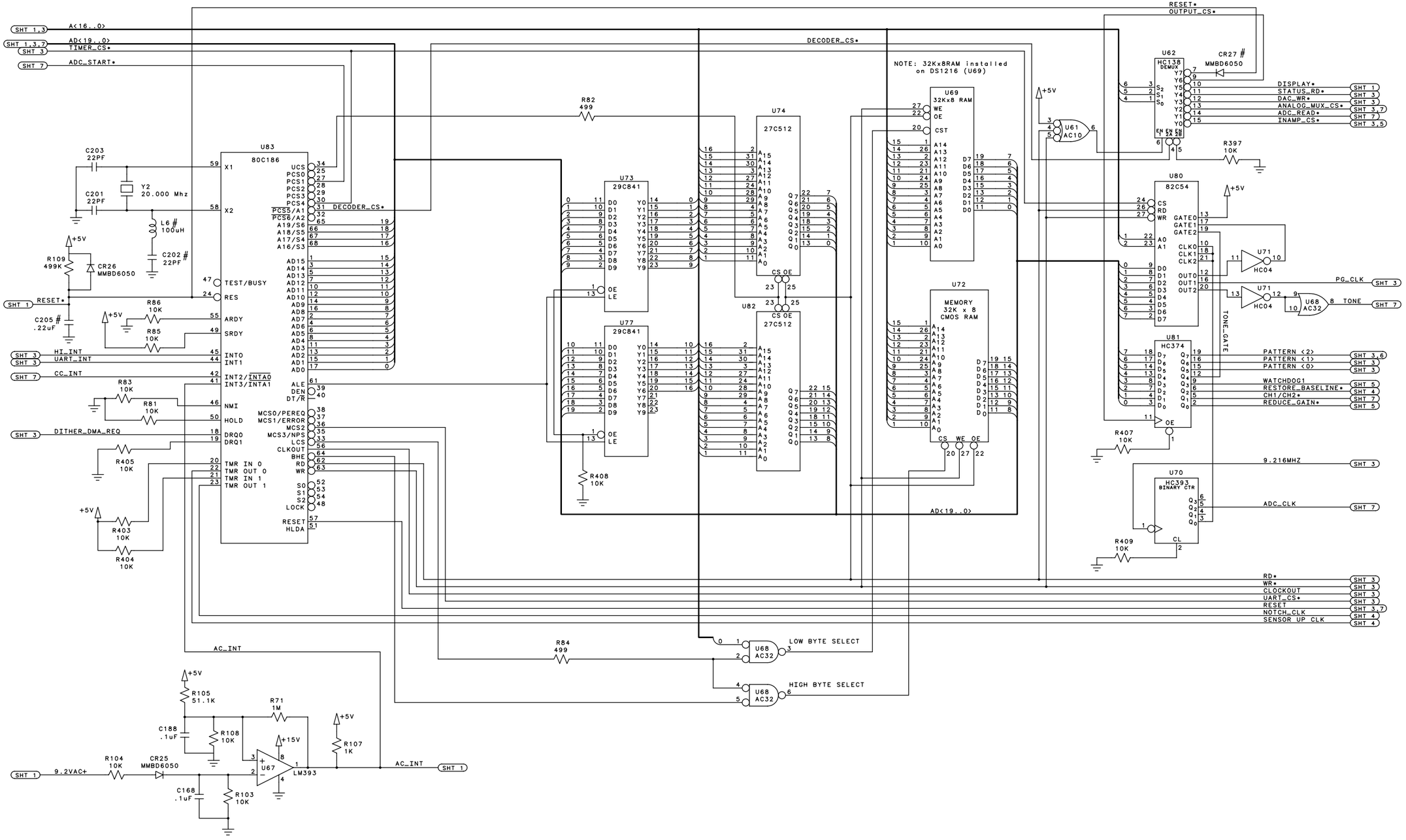
DESIGNATOR	PART TYPE	AGND	AGNDC	GND	-15V	+5VC	+15V	+5VA	+5V
U1	74HC573		10			20			
U2,U5,U85	74HC244		10			20			
U3,U10,U62	74HC138		8			16			
U4	82C53		14			28			
U7	80C85A		23			44			
U8	RAM8K8		14			28			
U9	74HC32		7			14			
U11,U22	82C51A		4			26			
U19	DS1232		8			15			
U20	27C256		16			32			
U33,U40,U41	DG403	13			14		11	12	
U52,U54	DG444	5			4		13	12	
U56	74HC161			8					16
U57,U59	74HC595			8					16
U58,U81	74HC374			10					20
U60,U73,U77	29C841			12					24
U61	74AC10			7					14
U62	74HC138			8					16
U64	27C256			16					32
U65	74HCT374			10					20
U68	74AC32			7					14
U69	DS1216			14					28
U70	74HC393			7					14
U71	74HC04			7					14
U72	55257			14					28
U74,U82	27C512			16					32
U45,U75,U79	74HC74			7					14
U76	74HC590			8					16
U80	82C54			14					28
U83	80C186			26,60					9,43
U84	82510			7					21
U85	74HC244			10					20
VR1	2940		4						

NOTES:

1. ALL RESISTORS ARE 1/8W 1% UNLESS SPECIFIED OTHERWISE.
2. ALL CAPACITORS ARE 50V UNLESS SPECIFIED OTHERWISE.
3. REFERENCE DESIGNATORS FOLLOWED BY "#" ARE NOT INSTALLED ON PCBA.
4. FOR COMPONENTS U52 AND U54 DG211 IS AN ACCEPTABLE SUBSTITUTE FOR THIS APPLICATION.

042839

Figure 4
Processor PCB Schematic (Sheet 1 of 13)



042839

Figure 4
Processor PCB Schematic (Sheet 2 of 13)

#NOTE:
W13 NOT INSTALLED ON PCBA.
W13 STRAPPED WITH ETCH ON PCB FAB.

NOTE:
JUMPER BLOCK W14 IDENTIFIES PEAK CURRENT TO LED DRIVE.
INSTALLED = 71mA; REMOVED = 84mA.
JUMPER BLOCK W14 MUST NOT BE INSTALLED.

042839

Figure 4
Processor PCB Schematic (Sheet 3 of 13)

#NOTE:
R70, C165 NOT INSTALLED ON PCBA.
PINS 1 AND 2 OF W8 STRAPPED WITH ETCH ON PCB FAB.

#NOTE:
COMPONENTS WITHIN DOTTED AREA NOT INSTALLED ON PCBA.

042839

Figure 4
Processor PCB Schematic (Sheet 4 of 13)

#NOTE:

C105, Q11, Q13, Q16, Q17, R68, R330, R337, R392, R395, W9, W10, W11, W12, W18, W19 NOT INSTALLED ON PCBA.

W9, W10 STRAPPED WITH ETCH ON PCB FAB.

PINS 1 AND 2 OF W11, W18, W19 STRAPPED WITH ETCH ON PCB FAB.

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Figure 4
Processor PCB Schematic (Sheet 5 of 13)

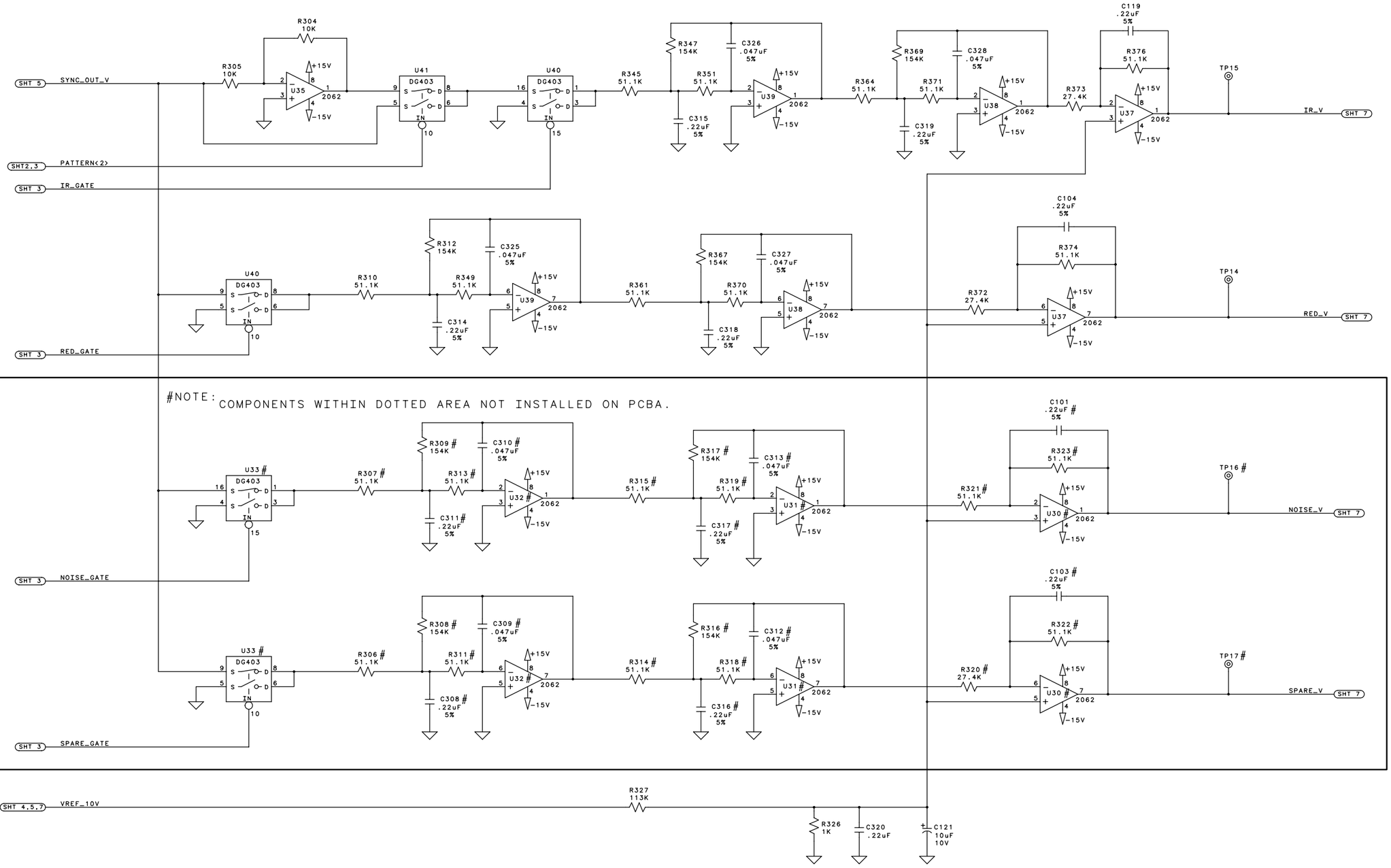

Figure 4
Processor PCB Schematic (Sheet 6 of 13)

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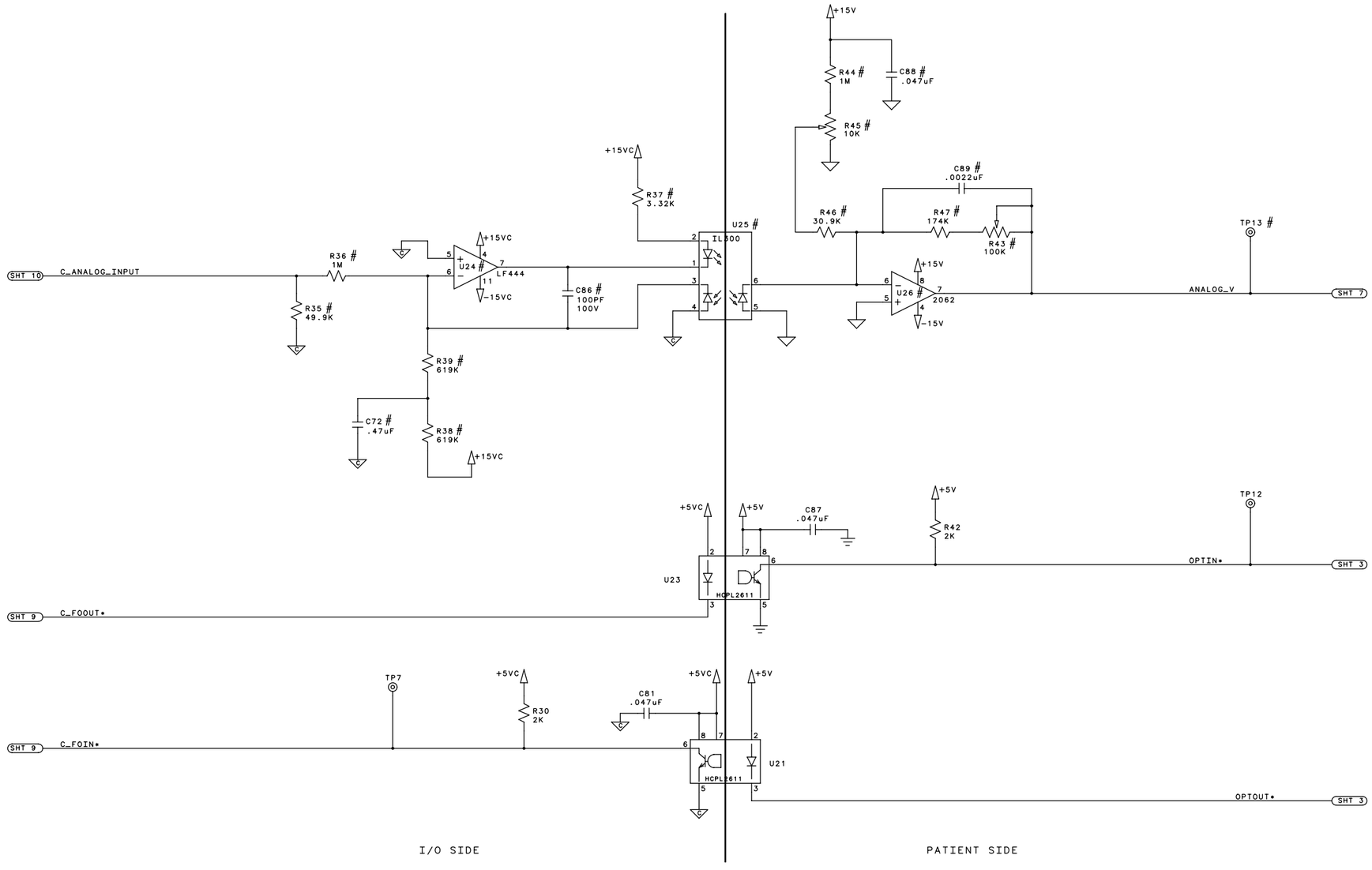
#NOTE:
R382, U27, W7 NOT INSTALLED ON PCBA.

042839

Figure 4
Processor PCB Schematic (Sheet 7 of 13)

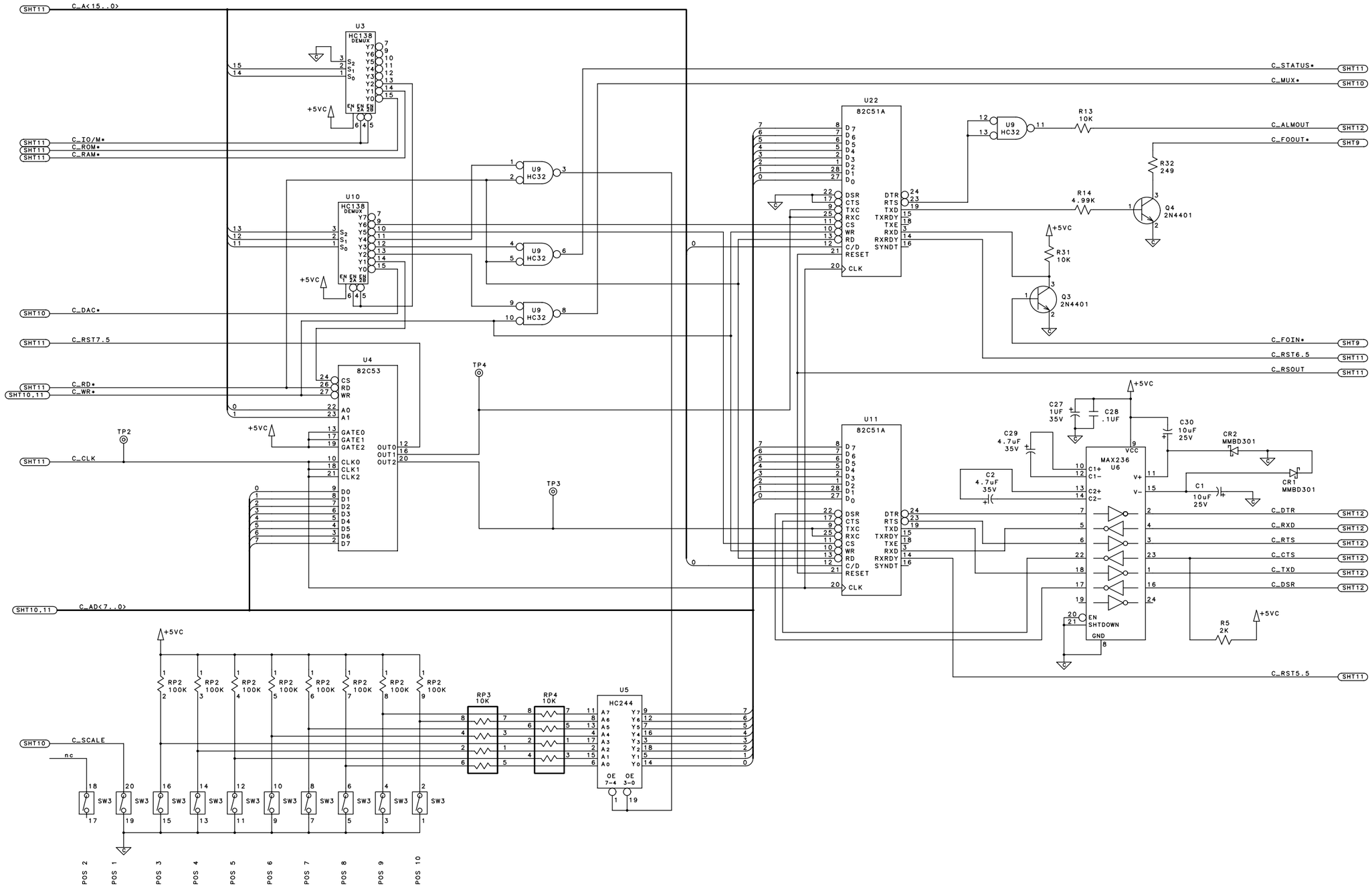
#NOTE:
C72, C86, C88, C89, R35, R36, R37, R38, R39, R43, R44,
R45, R46, R47, TP13, U24, U25, U26 NOT INSTALLED ON PCBA.



INTERNAL INTERFACE

042839

Figure 4
Processor PCB Schematic (Sheet 8 of 13)



042839

Figure 4
Processor PCB Schematic (Sheet 9 of 13)

#NOTE:
C12, C13, C14, C15, J12 NOT INSTALLED ON PCBA.

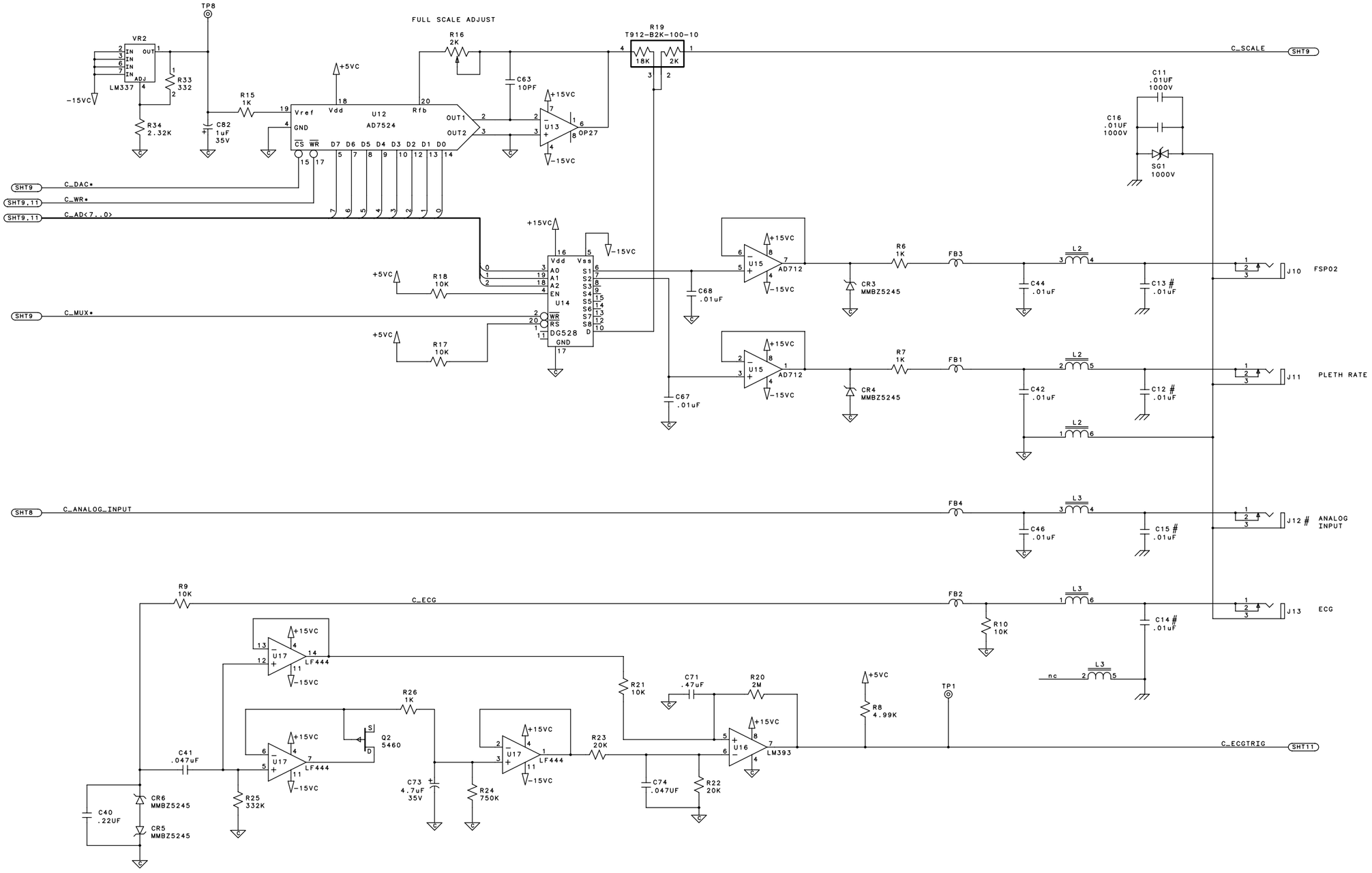


Figure 4
Processor PCB Schematic (sheet 10 of 13)

042839

#NOTE:
W1, W2, W3, W4, W5, W6 NOT INSTALLED ON PCBA.
W1 STRAPPED WITH ETCH ON PCB FAB.
PINS 2 AND 3 OF W6 STRAPPED WITH ETCH ON PCB FAB.

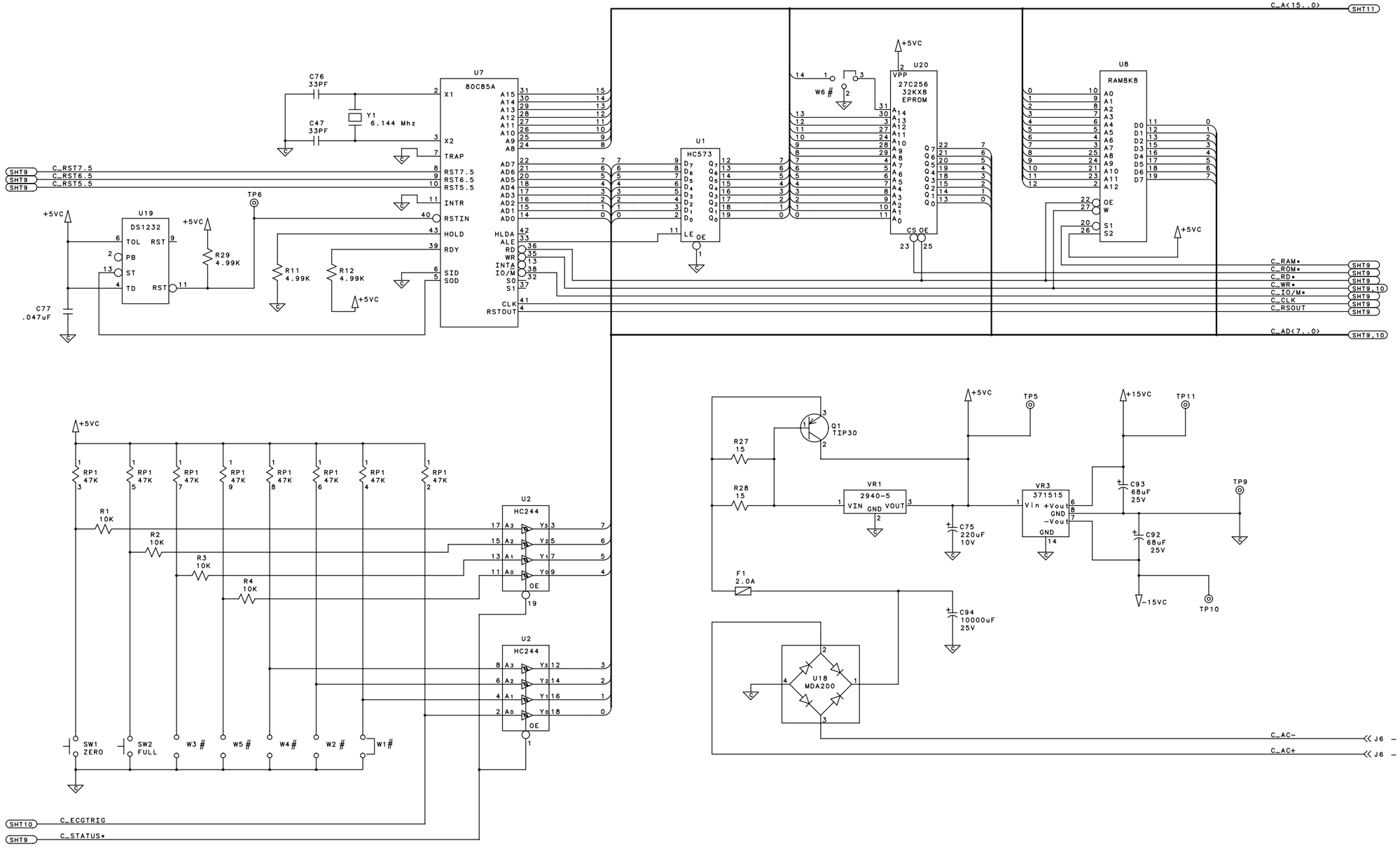
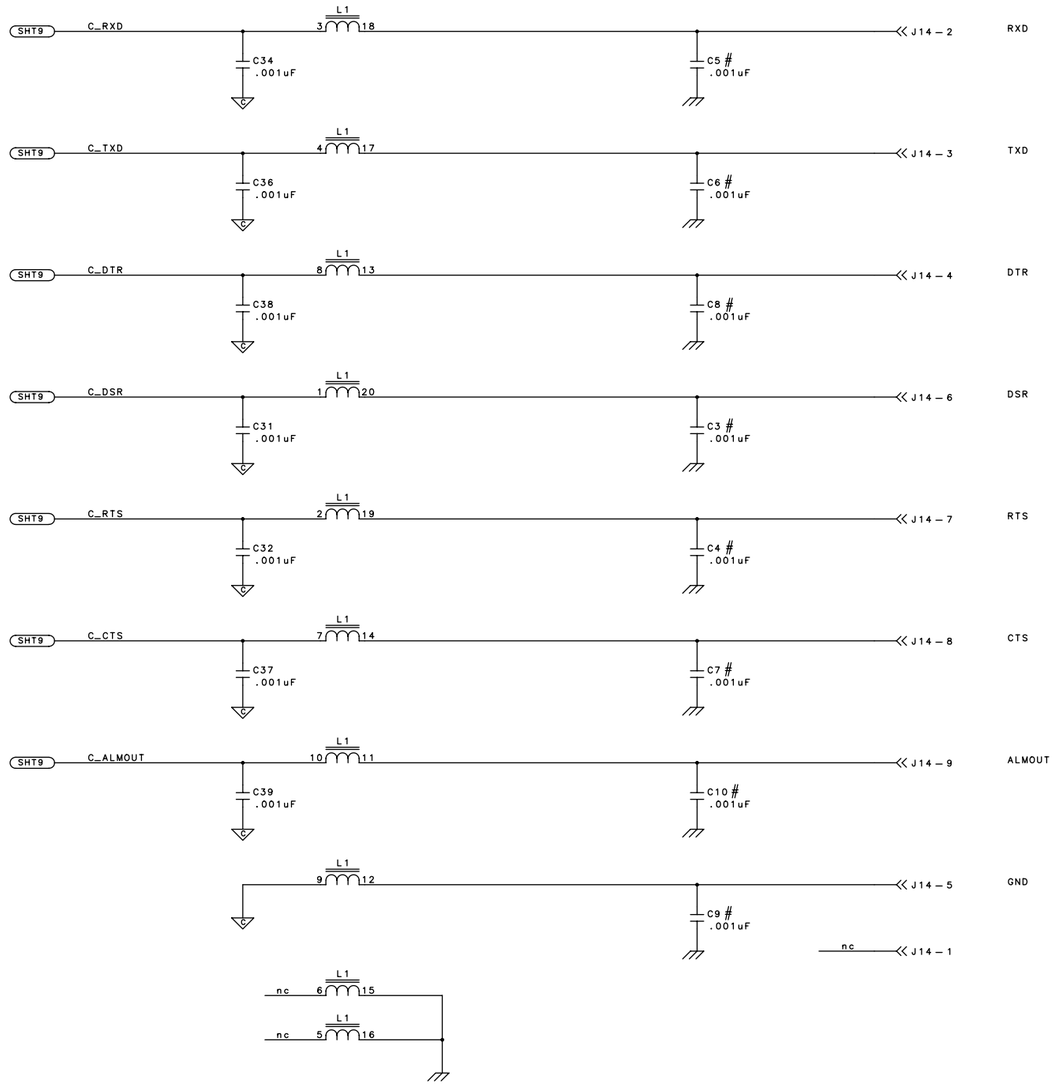


Figure 4
Processor PCB Schematic (Sheet 11 of 13)

042839

#NOTE:
C3, C4, C5, C6, C7, C8, C9, C10 NOT INSTALLED ON PCBA.



GH10, GH11 REPRESENT MOUNTING HOLES ON PCB FAB FOR CONN J14.

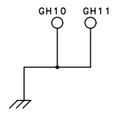
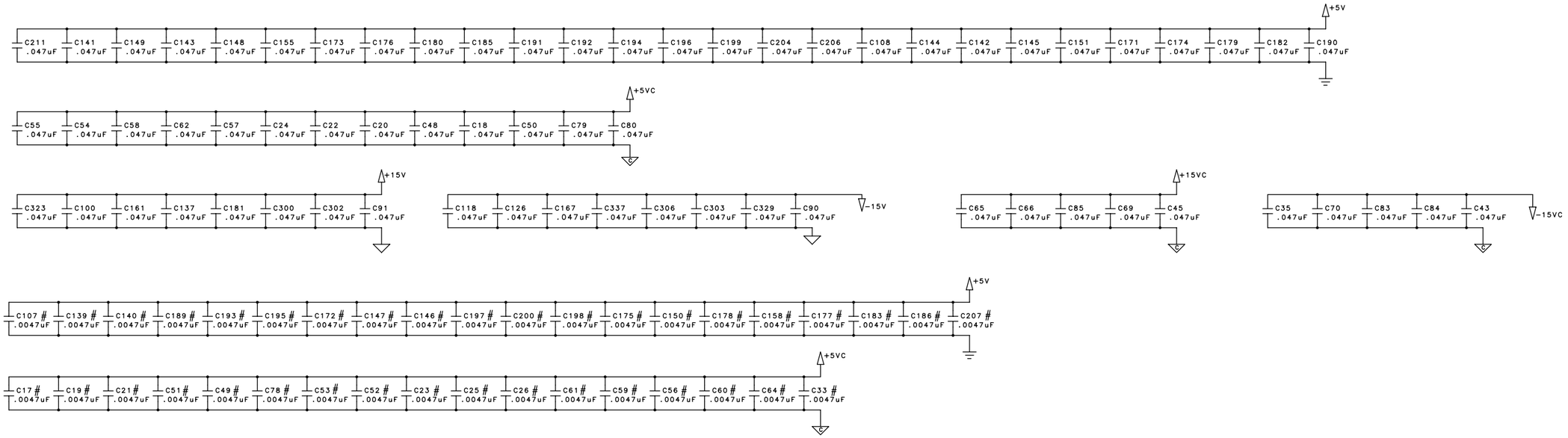


Figure 4
Processor PCB Schematic (Sheet 12 of 13)

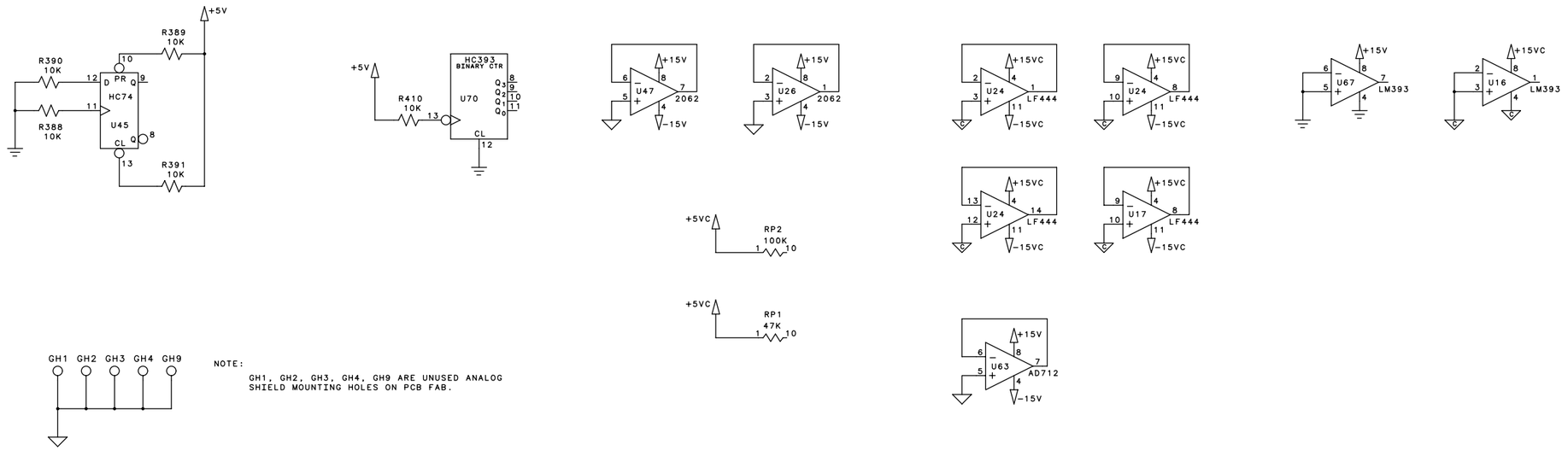
042839

#NOTE:
.0047UF CAPACITORS NOT INSTALLED ON PCBA.

BYPASS CAPACITORS



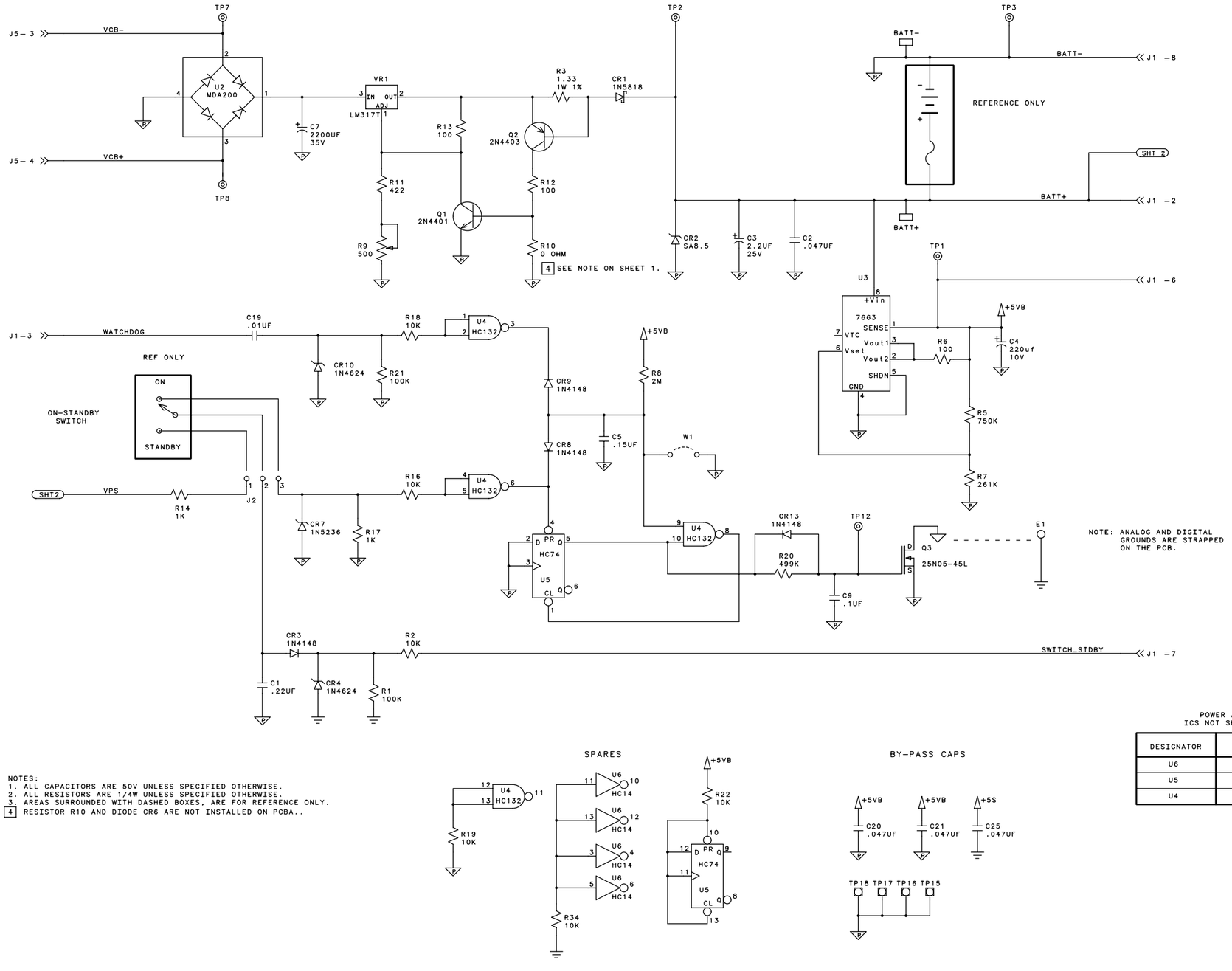
SPARES



NOTE:
GH1, GH2, GH3, GH4, GH9 ARE UNUSED ANALOG SHIELD MOUNTING HOLES ON PCB FAB.

042839

Figure 4
Processor PCB Schematic (Sheet 13 of 13)



NOTES:
1. ALL CAPACITORS ARE 50V UNLESS SPECIFIED OTHERWISE.
2. ALL RESISTORS ARE 1/4W UNLESS SPECIFIED OTHERWISE.
3. AREAS SURROUNDED WITH DASHED BOXES, ARE FOR REFERENCE ONLY.
4. RESISTOR R10 AND DIODE CR6 ARE NOT INSTALLED ON PCBA..

POWER AND GROUND CONNECTIONS FOR
ICS NOT SHOWN EXPLICITLY ON THE SCHEMATIC

DESIGNATOR	PART TYPE	PGND	GND	+5VB	+5S
U6	74HC14		7		14
U5	74HC74	7		14	
U4	74HC132	7		14	

023084

Figure 5
Power PCB Schematic (Sheet 1 of 2)

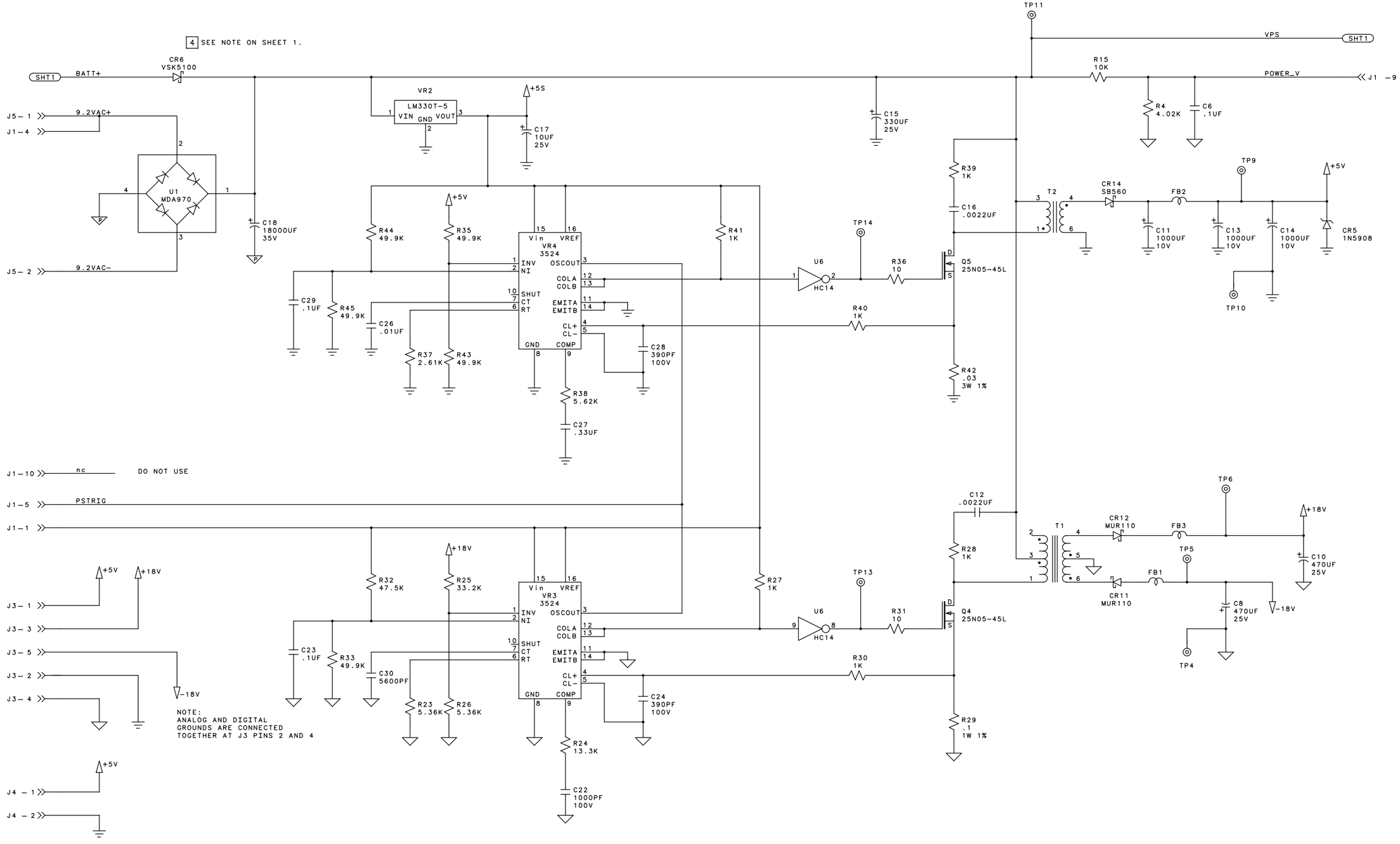
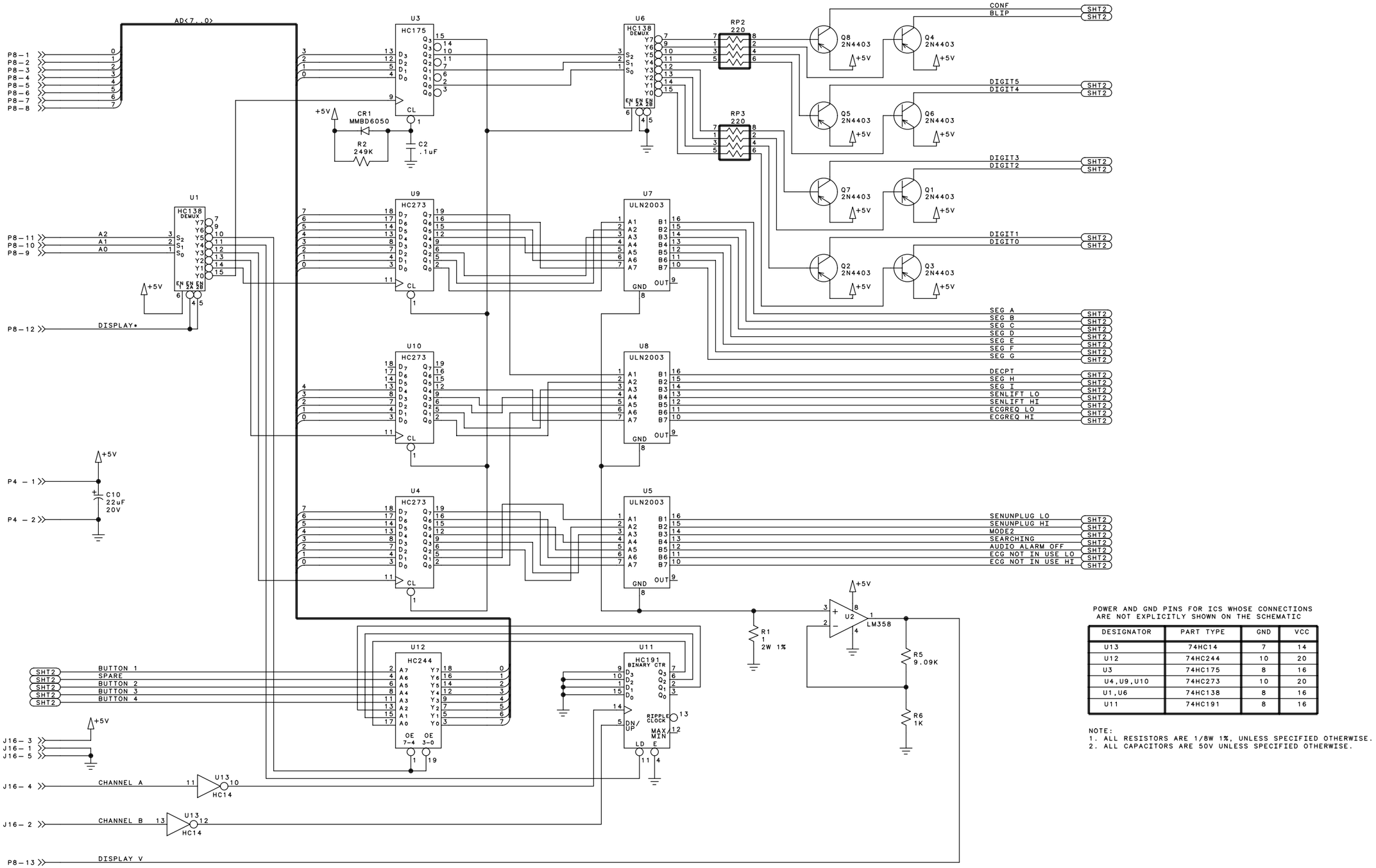


Figure 5
Power PCB Schematic (Sheet 2 of 2)

023084



POWER AND GND PINS FOR ICS WHOSE CONNECTIONS ARE NOT EXPLICITLY SHOWN ON THE SCHEMATIC

DESIGNATOR	PART TYPE	GND	VCC
U13	74HC14	7	14
U12	74HC244	10	20
U3	74HC175	8	16
U4,U9,U10	74HC273	10	20
U1,U6	74HC138	8	16
U11	74HC191	8	16

NOTE:
1. ALL RESISTORS ARE 1/8W 1%, UNLESS SPECIFIED OTHERWISE.
2. ALL CAPACITORS ARE 50V UNLESS SPECIFIED OTHERWISE.

Figure 6
Display PCB Schematic (Sheet 1 of 2)

023064

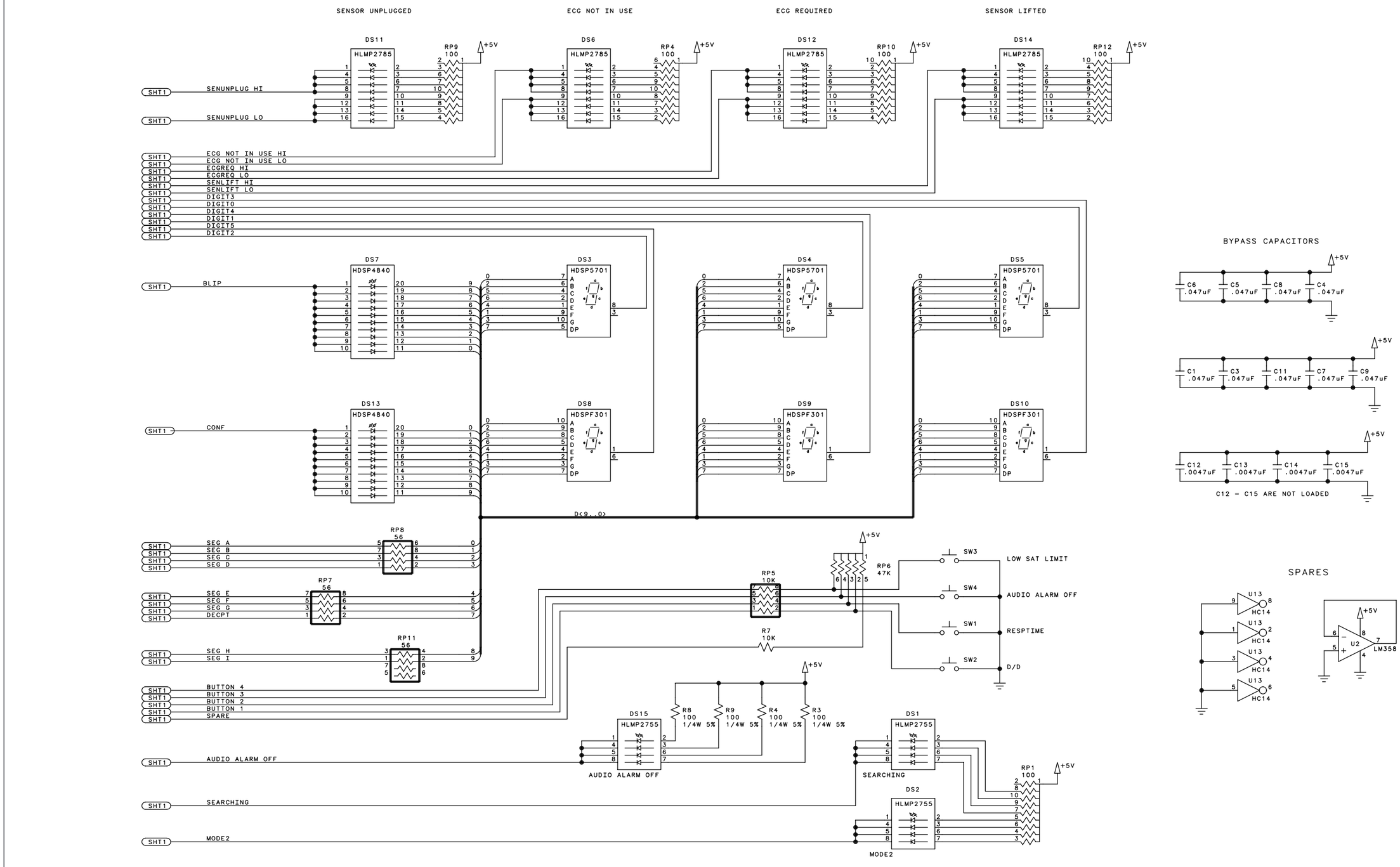
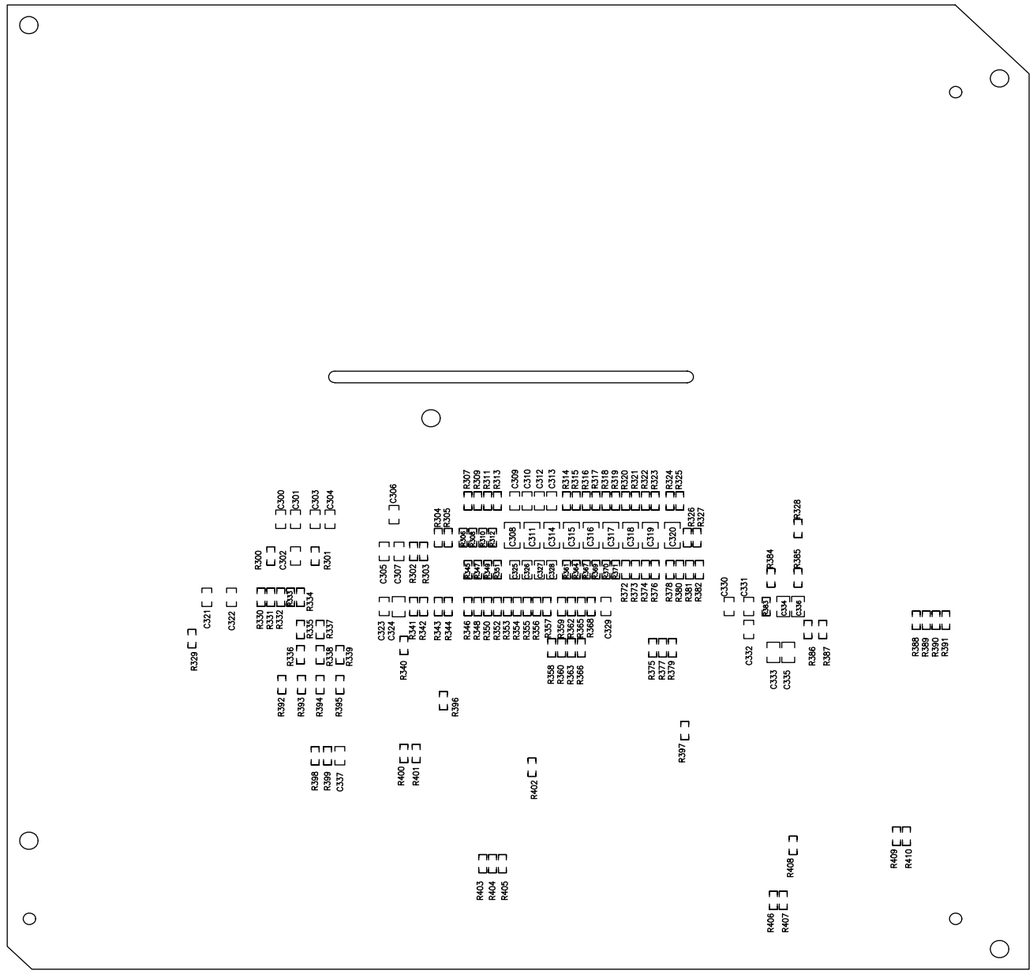
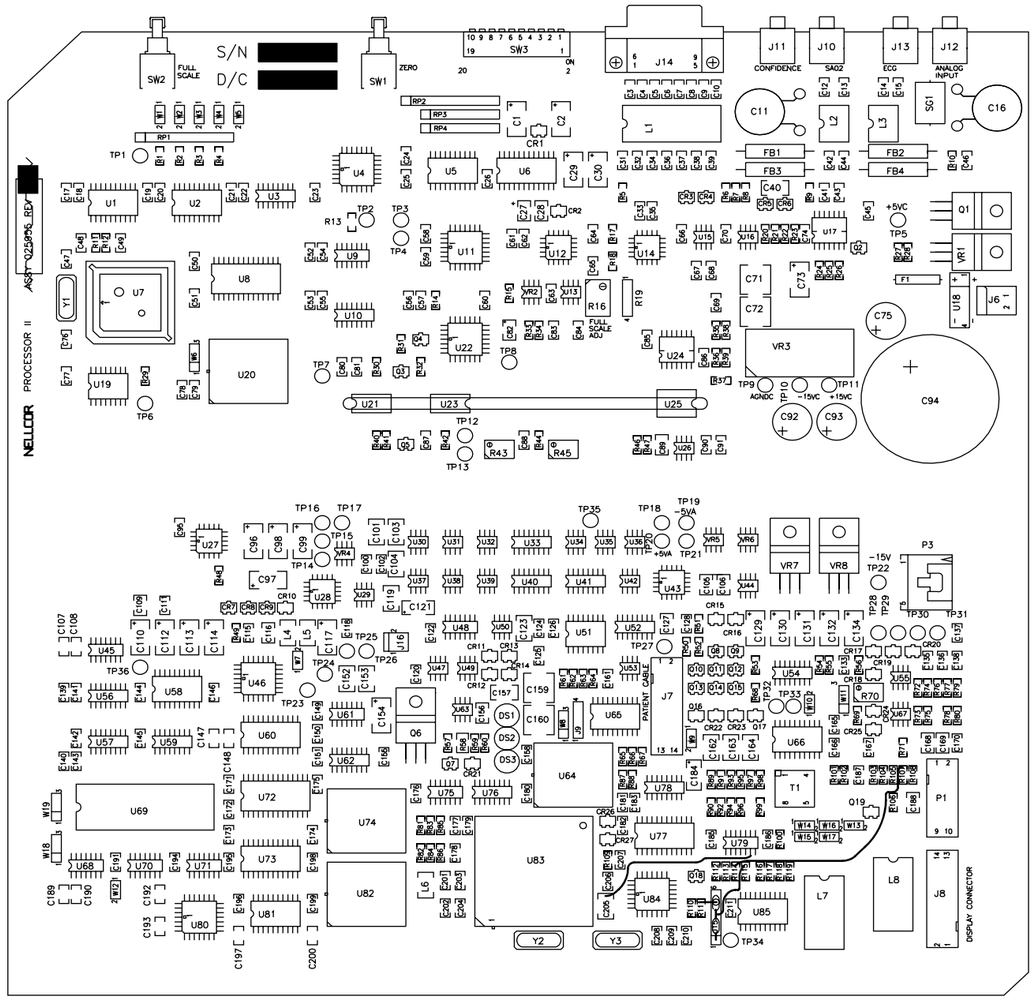


Figure 6
Display PCB Schematic (Sheet 2 of 2)

023064



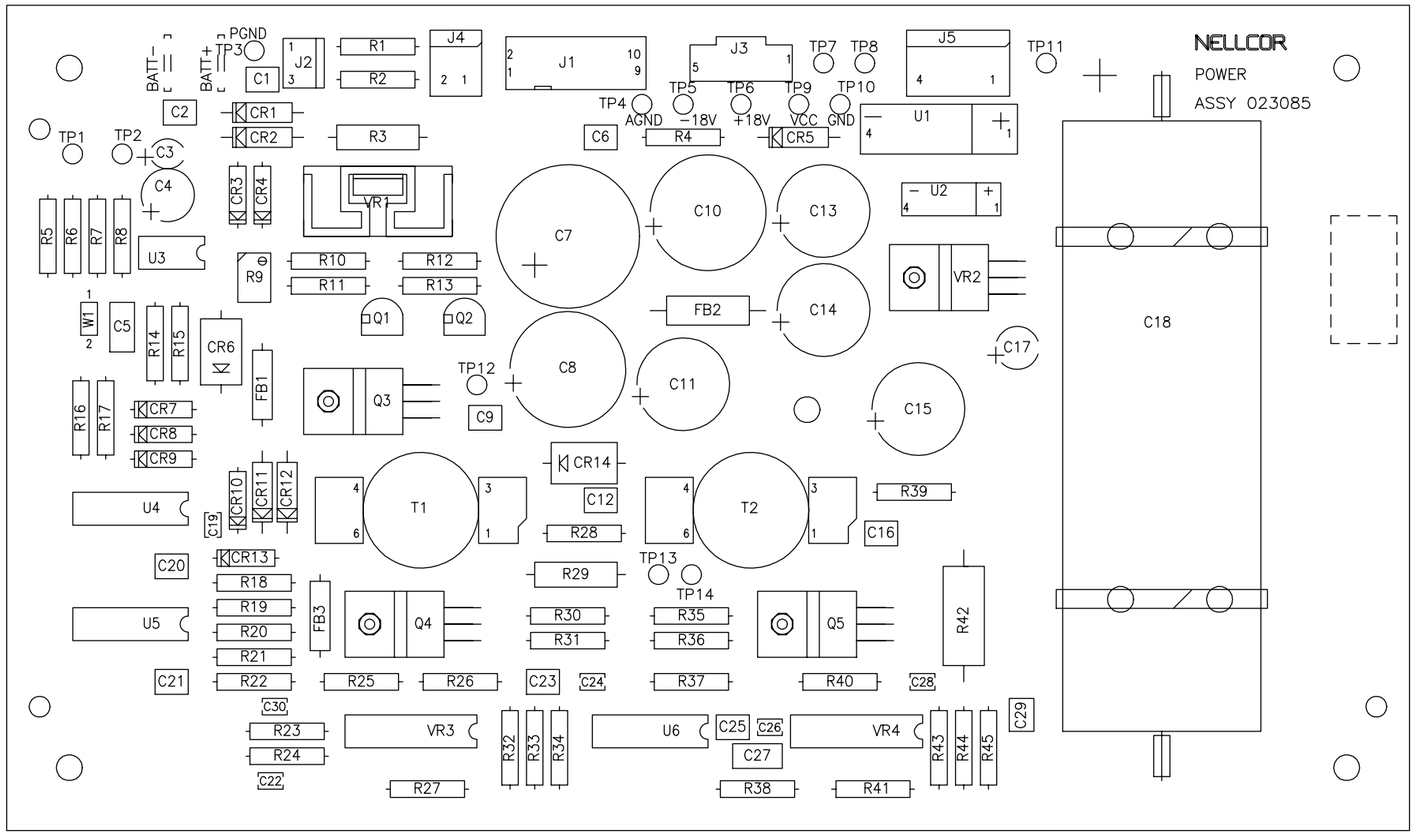
SECONDARY SIDE



PRIMARY SIDE

042840

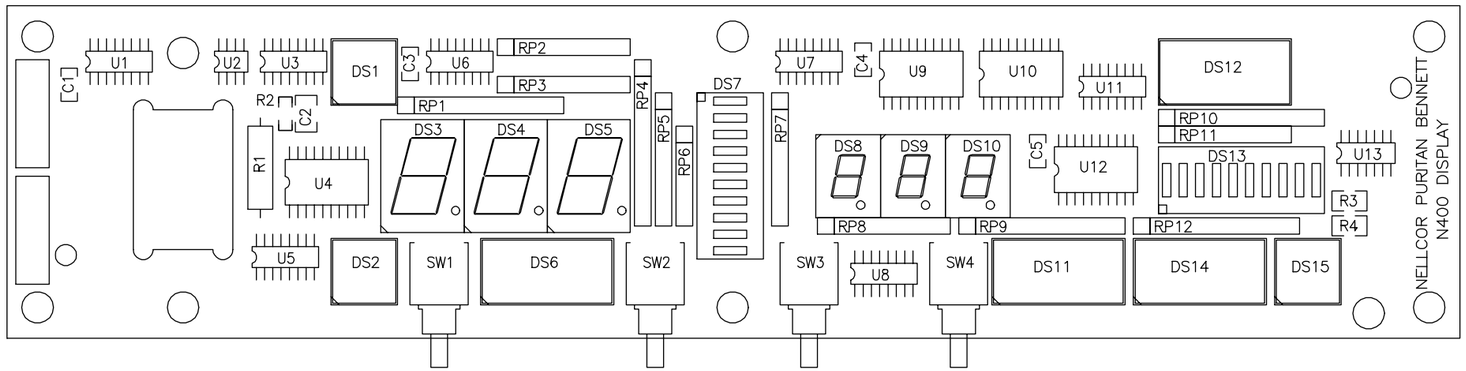
Figure 7
Processor PCB Assembly



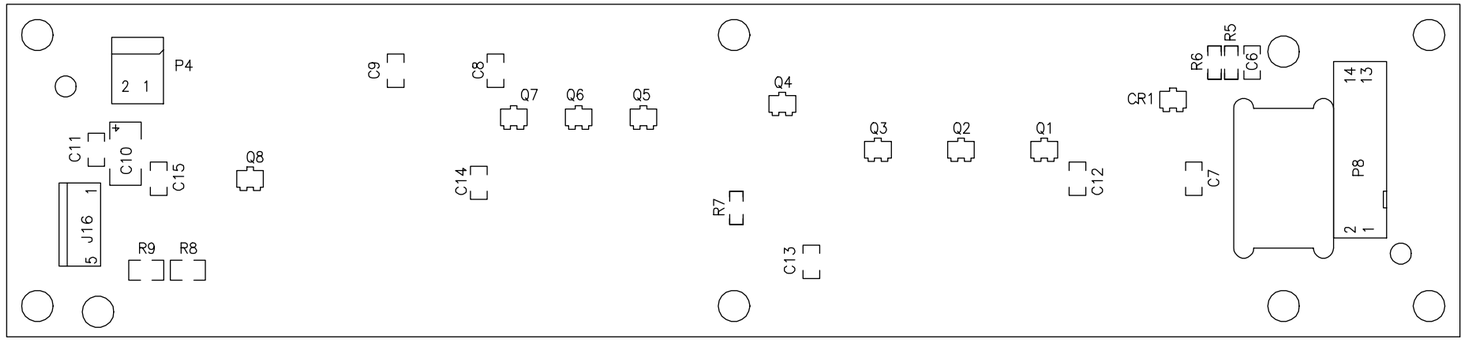
COMPONENT SIDE

Figure 8
Power PCB Assembly

023085



PRIMARY SIDE



SECONDARY SIDE

Figure 9
Display PCB Assembly

023065

Nellcor

Tyco Healthcare Group LP
Nellcor Puritan Bennett Division
4280 Hacienda Drive
Pleasanton, CA 94588 U.S.A.
Telephone Toll Free 1.800.NELLCOR

Authorized Representative
Tyco Healthcare UK LTD
154 Fareham Road
Gosport PO13 0AS, U.K.

Rx ONLY

CE
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